

***LCFC FL490/FL590 NM-B931***

***Solo/Lando 2.0***


***NM-XXXX Rev 1.0 Schematic***

***Intel Whiskey Processor with DDR4 + PCH***

***AMD R18M-M2-60***

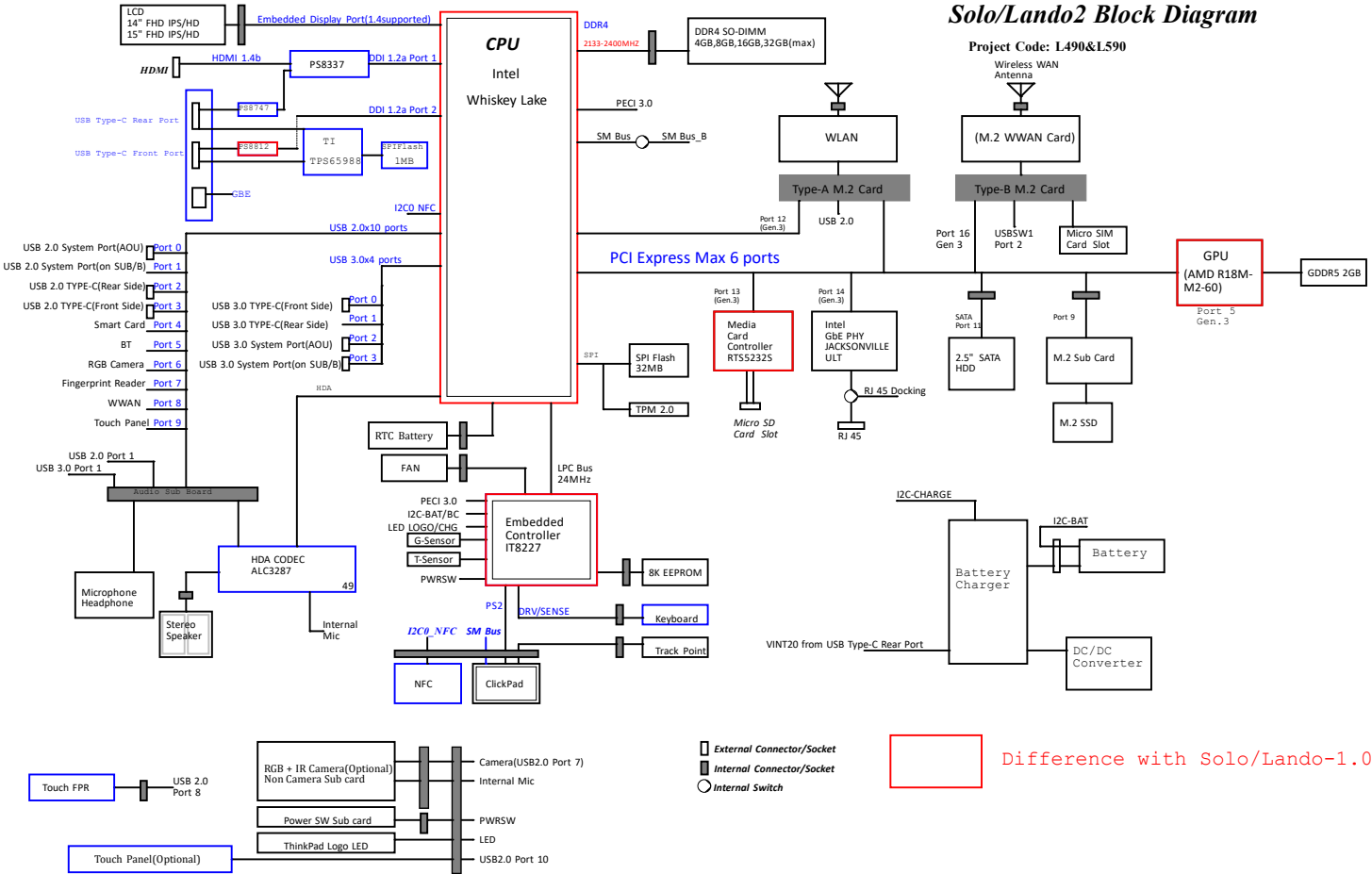
***2018-09-26 Rev 0.3***

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Rev 0.3

Solo/Lando2 Block Diagram



## Voltage Rails

O --> Means ON  
X --> Means OFF

Power Plane / State	B+	+1.05VALW +3VALW +1.8VALW +5VALW	+1.2V +0.6VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL							
	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#	SYSON
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	OFF	ON	OFF	HIGH
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	OFF	ON	OFF	LOW
S5 (Soft OFF)	LOW	LOW	LOW	LOW	OFF	ON	OFF	LOW

## SMBUS Control Table

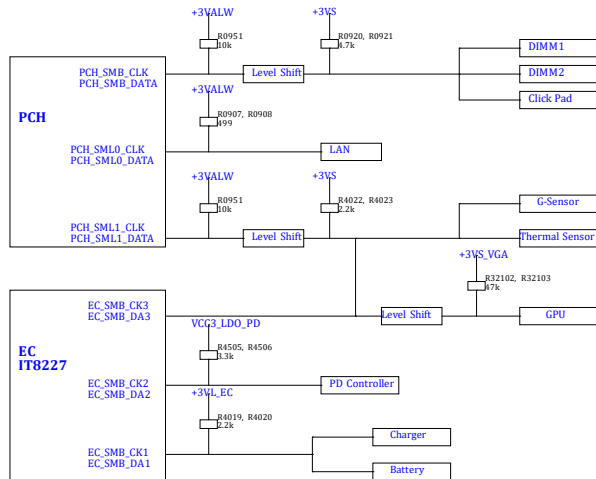
	SOURCE	Main VGA	BATT	SODIMM	Thermal Sensor	PCH	CP Module	LAN PHY	G-Sensor	EC
EC_SMB_CK1 EC_SMB_DA1	IT8227 +3VL_EC	X	V +3VL_EC	X	X	X	X	X	X	V +3VL_EC
EC_SMB_CK2 EC_SMB_DA2	IT8227 VCC3_LDO_PD	X	X	X	X	X	X	X	X	V VCC3_LDO_PD
EC_SMB_CK3 EC_SMB_DA3	IT8227 +3VS	V +3VS_VGA	X	X	V +3VS	V +3VALW_PCH	X	X	V +3VS	V +3VS
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	V +3VS	X	V +3VALW_PCH	V +3VS	X	X	X
PCH_SML0_CLK PCH_SML0_DATA	PCH +3VALW_PCH	X	X	X	X	V +3VALW_PCH	X	V +3VALW	X	X
PCH_SML1_CLK PCH_SML1_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VALW_PCH	X	X	V +3VS	V +3VS

## HSIO Port

Port	Device
1	TYPE-C(Front Side)
2	TYPE-C(Rear Side)
3	System Port(AOU)
4	System Port on SUB/B
5	PCIE (GPU)
6	PCIE (GPU)
7	PCIE (GPU)
8	PCIE (GPU)
9	NVMe SSD
10	NVMe SSD
11	2.5" SATA HDD
12	PCIE (WLAN)
13	Card Reader
14	LAN
15	M.2 (PCIE)
16	M.2 (SATA)

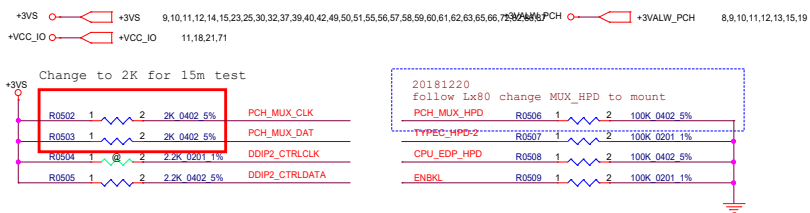
## USB2.0 Port

Port	Device
1	USB Port1 ( AOU)
2	USB Port2 (SUB/B)
3	USB Port3 (TYPE-C)
4	USB Port4 (TYPE-C CS18 DOCK)
5	SMART Card
6	BT
7	RGB USB CAMERA
8	Finger Printer
9	WWAN
10	Touch panel

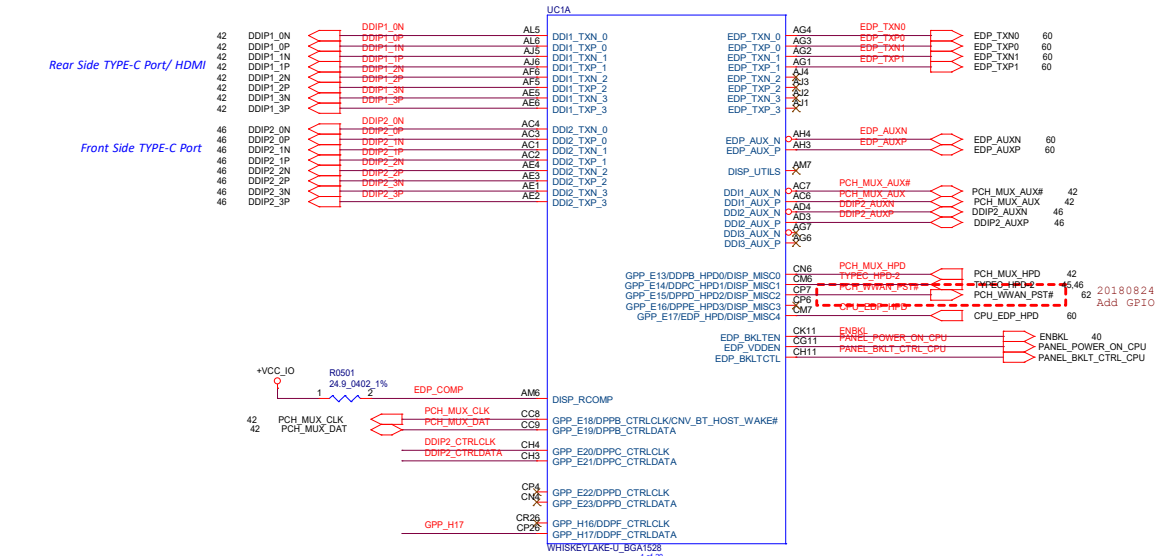


**BOM Structure Table**

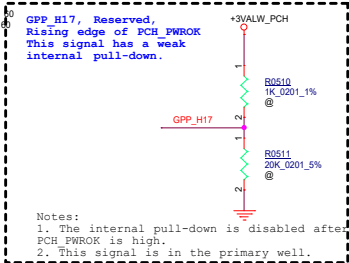
BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function with WWAN
DIS@	Discreate SKU
UMA@	UMA SKU
SATA_RE@	With SATA re-driver
NSATA_RE@	Bypass SATA re-driver
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
MIRROR@	For mirror function
TPM@	TPM function
NTPM@	Non TPM function
X76@	GPU VRAM Setting
DCI@	DCI function
ME@	ME Connector
EMC@	For EMC function
EMC_NS@	For EMC function (no mount)
RF@	For RF function
RF_NS@	For RF function (no mount)
Audio@	For Non Audio debug function
SW@	For Audio debug function
CRR@	For Card reader REALTEK strap
CRG@	For Card reader BayHub strap



DP port	Enable	Disable
DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm$ 5% resistor	no connect
DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm$ 5% resistor	no connect



**EDP\_RCOMP**  
1. Trace width=20mils, Spacing=25mils, Max length=600mils  
2. RCL close to MCP  
Trace Width=20mil, Spacing=25mil, Max length=600mil  
Pull-up to VCCIO through 24.9- $\Omega$   $\pm$  1% resistor  
For CNL, it is 100  $\Omega$   $\pm$  1%  
Please refer to PDG Table 3-2.



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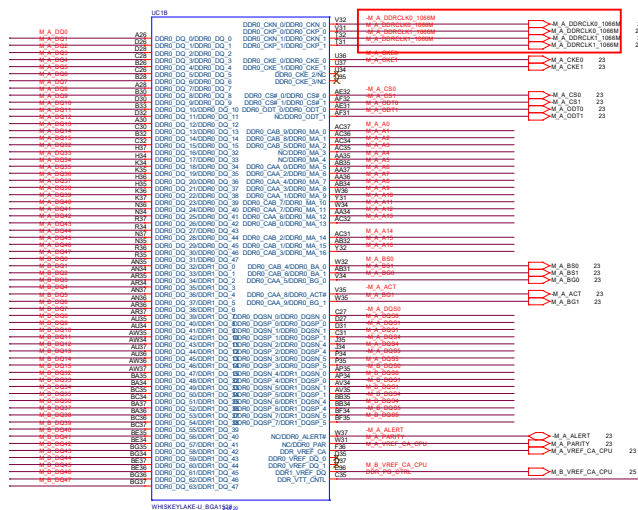
Title		WHL(A)_DDI/EDP	
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TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
Block 2	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
Block 6	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 8	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
Block 10	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BA27	DDR0_DQ[60]	DDR1_DQ[44]
	BA25	DDR0_DQ[61]	DDR1_DQ[45]
	BB25	DDR0_DQ[62]	DDR1_DQ[46]
	BA23	DDR0_DQ[63]	DDR1_DQ[47]
	BB23	DDR0_DQ[64]	DDR1_DQ[48]
	AY21	DDR0_DQ[65]	DDR1_DQ[49]
	AW21	DDR0_DQ[66]	DDR1_DQ[50]
	BA21	DDR0_DQ[67]	DDR1_DQ[51]

↑  
LOGIC



TABLE

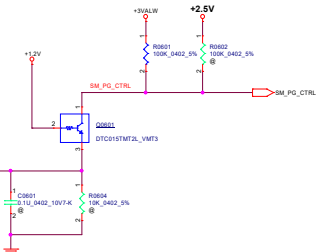
	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT69	DDR0_DQSN[2]	DDR0_DQSN[2]
	AT70	DDR0_DQSN[3]	DDR0_DQSN[3]
Block 2	BA64	DDR0_DQSN[4]	DDR0_DQSN[4]
	AY64	DDR0_DQSN[5]	DDR0_DQSN[5]
	AY60	DDR0_DQSN[6]	DDR0_DQSN[6]
	BA60	DDR0_DQSN[7]	DDR0_DQSN[7]
Block 4	BA38	DDR0_DQSN[8]	DDR0_DQSN[8]
	AY38	DDR0_DQSN[9]	DDR0_DQSN[9]
	AY34	DDR0_DQSN[10]	DDR0_DQSN[10]
	BA34	DDR0_DQSN[11]	DDR0_DQSN[11]
Block 6	BA30	DDR0_DQSN[12]	DDR0_DQSN[12]
	AY30	DDR0_DQSN[13]	DDR0_DQSN[13]
	AY26	DDR0_DQSN[14]	DDR0_DQSN[14]
	BA26	DDR0_DQSN[15]	DDR0_DQSN[15]

↑  
LOGIC

TABLE

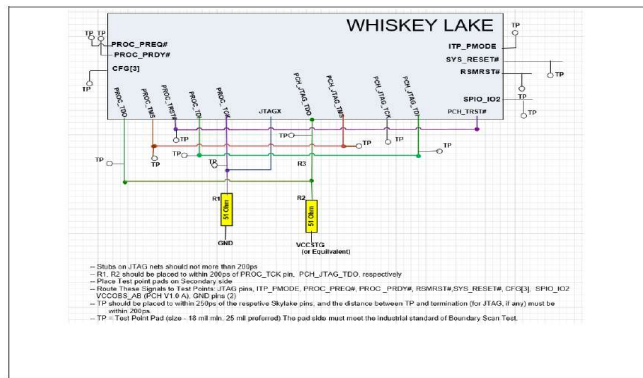
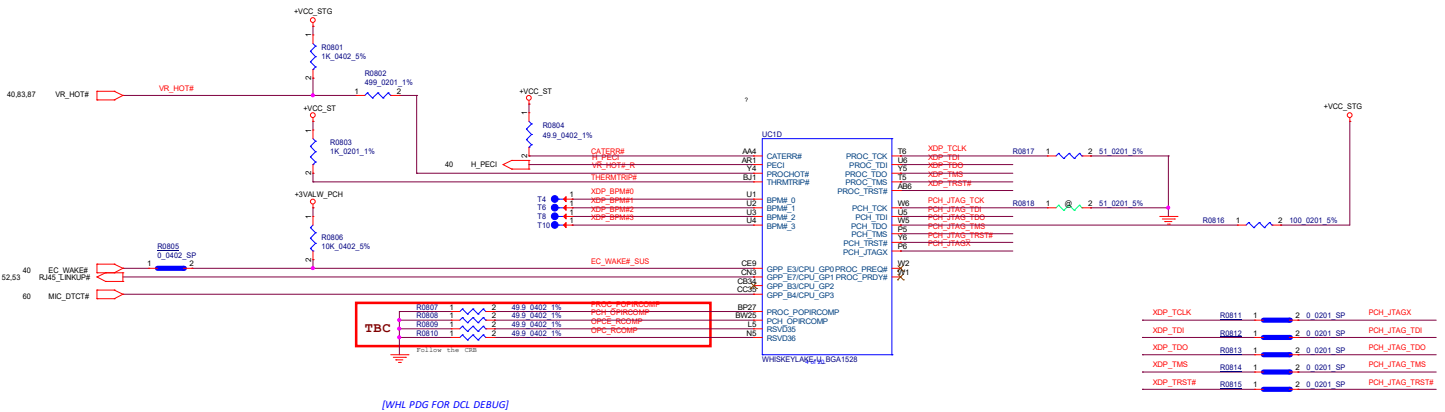
Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[6]	DDR0_CAA[1]	DDR0_MA[6]
BA52	DDR0_MA[7]	DDR0_CAA[2]	DDR0_MA[7]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[9]	DDR0_CAA[4]	DDR0_MA[9]
AY55	DDR0_MA[10]	DDR0_CAA[5]	DDR0_MA[10]
AW54	DDR0_MA[11]	DDR0_CAA[6]	DDR0_MA[11]
BA54	DDR0_MA[12]	DDR0_CAA[7]	DDR0_MA[12]
BA55	DDR0_MA[13]	DDR0_CAA[8]	DDR0_MA[13]
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_MA[14]
AU46	DDR0_MA[15]	DDR0_CAB[0]	DDR0_MA[15]
AU48	DDR0_MA[16]	DDR0_CAB[1]	DDR0_MA[16]
AT46	DDR0_MA[17]	DDR0_CAB[2]	DDR0_MA[17]
AU50	DDR0_MA[18]	DDR0_CAB[3]	DDR0_MA[18]
AU52	DDR0_MA[19]	DDR0_CAB[4]	DDR0_MA[19]
AY51	DDR0_MA[20]	DDR0_CAB[5]	DDR0_MA[20]
AT48	DDR0_MA[21]	DDR0_CAB[6]	DDR0_MA[21]
AT50	DDR0_MA[22]	DDR0_CAB[7]	DDR0_MA[22]
BB50	DDR0_MA[23]	DDR0_CAB[8]	DDR0_MA[23]
AY50	DDR0_MA[24]	DDR0_CAB[9]	DDR0_MA[24]
BA50	DDR0_MA[25]	DDR0_CAB[10]	DDR0_MA[25]
BB52	DDR0_MA[26]	DDR0_CAB[11]	DDR0_MA[26]

↑  
LOGIC





+VCC\_ST 15,16,18,71,97  
 +VCC\_STG 16,18,71  
 +3VALW\_PCH 5,8,10,11,12,13,15,19



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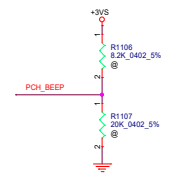
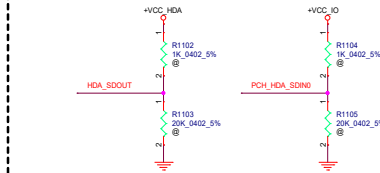
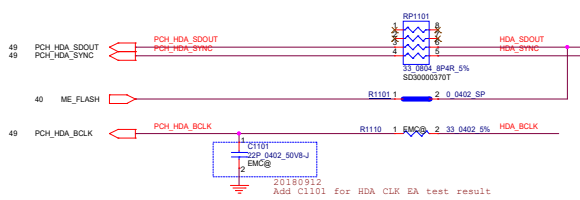




+3VALW\_PCH 5,8,9,10,12,13,15,19  
 +3VS 5,9,10,12,14,15,23,25,30,32,37,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,65,66,72,82,86,87  
 +VCC\_HDA 19  
 +VCC\_IO 5,18,21,71  
 +3VALW 6,8,10,12,13,15,18,19,39,40,41,43,45,46,48,52,58,60,62,63,65,66,67,71,72,83,84,85,96

To enable Flash Descriptor Security Override, this signal should be pulled up to VCC\_HDA through a 1 K $\Omega$  to 2.2 K $\Omega$   $\pm$  5% resistor

GPP\_B14, Internal PD 20K  
 No Reboot on TCO  
 Timer expiration  
 pull-up to VCC3\_3 through a 1-8.2K $\Omega$  resistor to disable this capability



WINDU and E470 can't stuff TBD

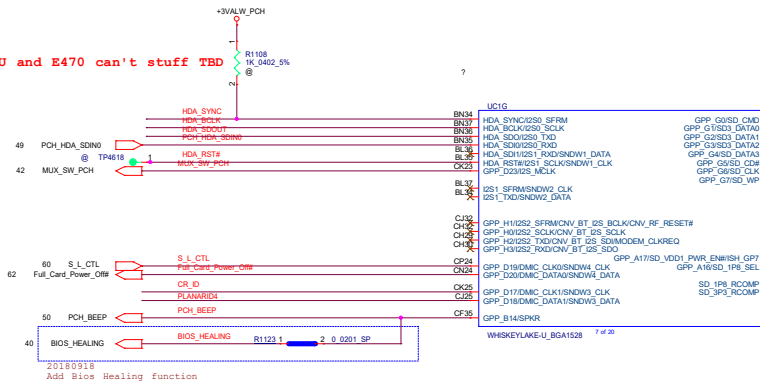


Table 3-1.RCOMP Recommendation for WHL and CFL

SD3 & EMHC	SD_1P8_RCOMP SD_3P3_RCOMP EMHC_RCOMP	2000 $\pm$ 1% to GND	<0.1	Notes: These pins can be merged into one 2000 $\pm$ 1% to GND resistor. Routing each of them to individual 2000 $\pm$ 1% to GND resistor is an option too.

Panel ID (Pin#2 Control)	TPM ID (GPP_D19)	Status	PLANARID4 (GPP_D18)	Status
15"	0 (GND Low)	TPM	0 (R1022)	
14"	1 (NC High)	NTPM	1 (R1021)	

Card Reader ID

Status	CR_ID (GPP_D17)
CRG	0 (R1022)
CRR	1 (R1021)

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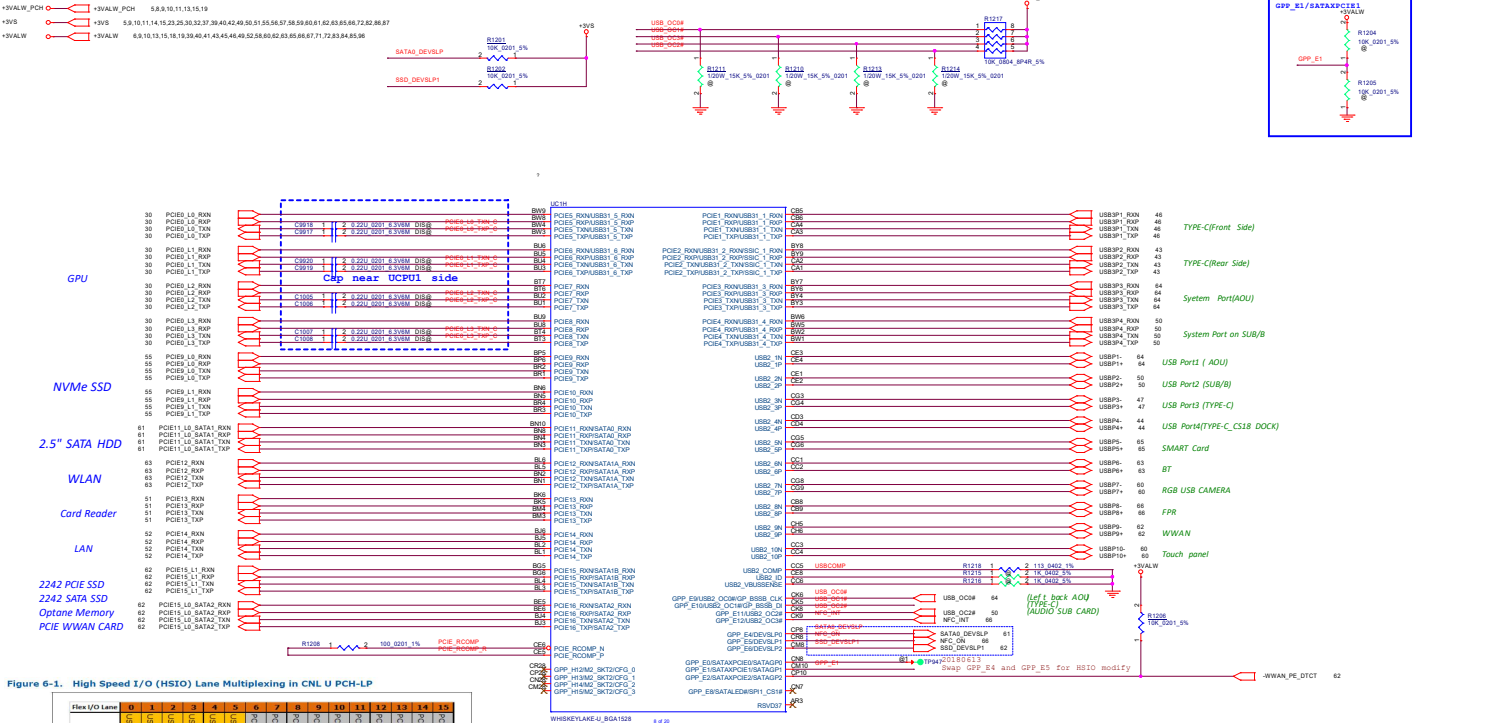


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-1P

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	PCIe #0	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15
Intel® RS5 Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support

Figure 6-2. Supported PCH PCI Express® Link Configurations

PCH-1P	PCIe* Controller #1		PCIe* Controller #2		PCIe* Controller #3				PCIe* Controller #4								
	Cycle Router #2								Cycle Router #3								
	Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Premium-U	PCIe* Lane	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	3x4	8P1				8P5				8P9				8P13			
	14x16	8P1				8P5				8P9				8P13			
	2x2	8P1	8P2	8P3	8P4	8P5	8P6	8P7	8P8	8P9	8P10	8P11	8P12	8P13	8P14	8P15	8P16
	4x4	8P1	8P2	8P3	8P4	8P5	8P6	8P7	8P8	8P9	8P10	8P11	8P12	8P13	8P14	8P15	8P16
	2x16	8P4	8P5	8P6	8P7	8P8	8P9	8P10	8P11	8P12	8P13	8P14	8P15	8P16	8P17	8P18	8P19
	2x16	8P4	8P5	8P6	8P7	8P8	8P9	8P10	8P11	8P12	8P13	8P14	8P15	8P16	8P17	8P18	8P19

HSIO Configuration	CS19 E14/E15
PCIe #1	Media Card Controller
PCIe #2	Type-C Port
PCIe #3	Type-A Port (SATA/AQU)
PCIe #4	Type-A Port (SATA/AQU)
PCIe #5	Type-A Port (SATA/AQU)
PCIe #6	Type-A Port (SATA/AQU)
PCIe #7	Type-A Port (SATA/AQU)
PCIe #8	Type-A Port (SATA/AQU)
PCIe #9	Type-A Port (SATA/AQU)
PCIe #10	Type-A Port (SATA/AQU)
PCIe #11	Type-A Port (SATA/AQU)
PCIe #12	Type-A Port (SATA/AQU)
PCIe #13	Type-A Port (SATA/AQU)
PCIe #14	Type-A Port (SATA/AQU)
PCIe #15	Type-A Port (SATA/AQU)
PCIe #16	Type-A Port (SATA/AQU)

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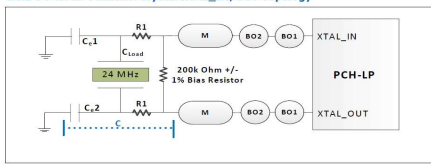
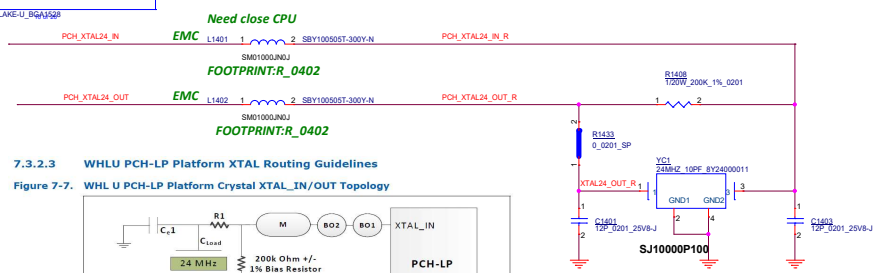
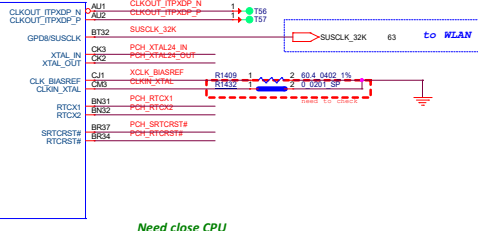
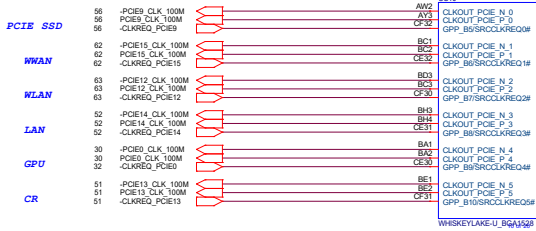
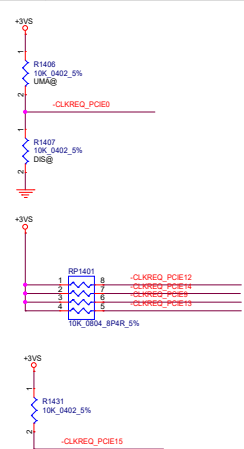
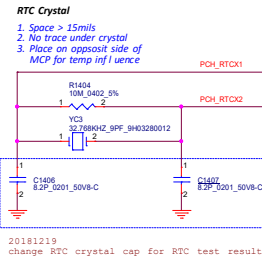
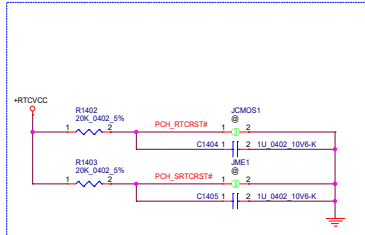
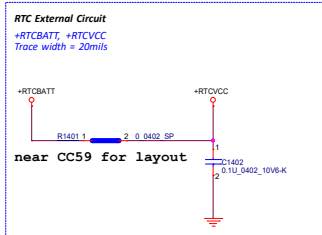
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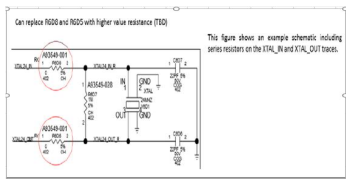


+RTCBATT 66.80  
+RTCVCC 15.19  
+3VS 5.9,10,11,12,15,23,25,30,32,37,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,65,66,72,82,86,87



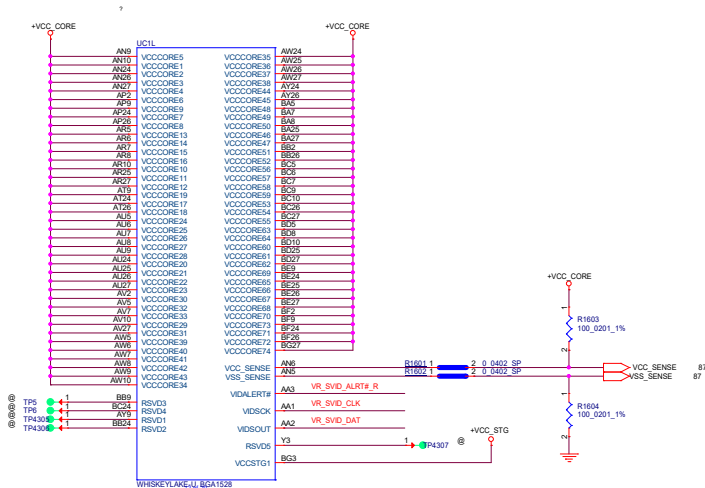
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	WHL(J)_RTC/CLK	
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				Quoted	FL490/FL590 NM-B931
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				Sheet	14 of 99
				Rev	0.3

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+VCC\_CORE 17,27,88,91  
+VCC\_ST 8,15,18,71,87  
+VCC\_STG 8,18,71

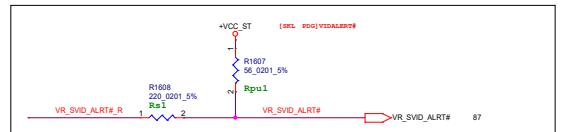
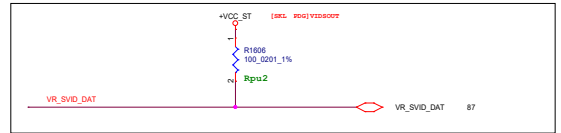
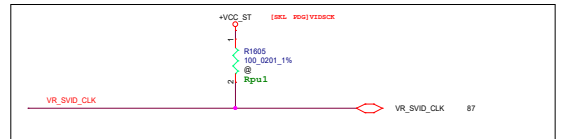


[WHL PDG] Package Sensing Recommendations

1. Trace Length Match: <25mil
2. Space: >25mil
3. Trace impedance: 50ohm
4. Sense traces should be referenced to a solid ground plane
5. Avoid crossing over plane splits

[WHL PDG] SVID

VIDALERT#, VIDSCCLK, and VIDSCCLK comprise a three signal serial synchronous interface (SVID) used to transfer power management information between the Whiskey Lake processor and the voltage regulator controllers. Alert signal must be routed between CLK and Data signals to minimize Cross-Talk.



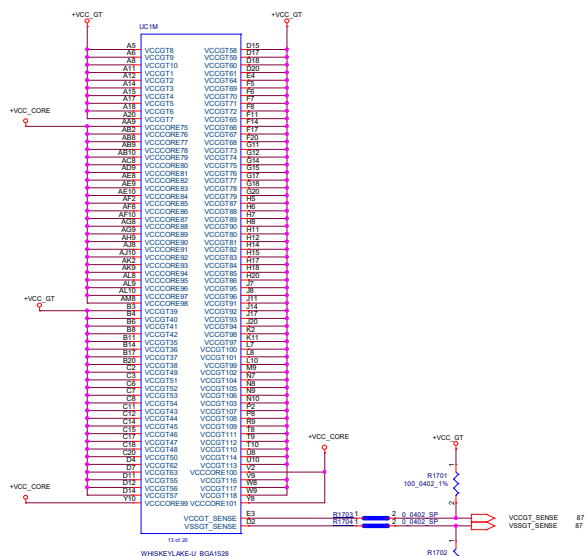
Topology Guidelines

SVID Signals	VIDSOUT, VIDSCCLK, VIDALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCCLK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

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				Date	Wednesday, March 11, 2015
				Sheet	15 of 99
				Rev	0.3



+VCC\_GT 27.88.91  
+VCC\_CORE 16.27.88.91



575414 WHL\_Ballout List

Pin Number	CPL U43e	WHL U42 QSP/Production	CNL U22/WHL U42 B301
A49	VCCGT	VCCGT	VCCGT
A50	VCCGT	VCCGT	VCCGT
A51	VCCGT	VCCGT	VCCGT
A52	VCCGT	VCCGT	VCCGT
A53	VCCGT	VCCGT	VCCGT
A54	VCCGT	VCCGT	VCCGT
A55	VCCGT	VCCGT	VCCGT
A56	VCCGT	VCCGT	VCCGT
A57	VCCGT	VCCGT	VCCGT
A58	VCCGT	VCCGT	VCCGT
A59	VCCGT	VCCGT	VCCGT
A60	VCCGT	VCCGT	VCCGT
A61	VCCGT	VCCGT	VCCGT
A62	VCCGT	VCCGT	VCCGT
A63	VCCGT	VCCGT	VCCGT
A64	VCCGT	VCCGT	VCCGT
A65	VCCGT	VCCGT	VCCGT
A66	VCCGT	VCCGT	VCCGT
A67	VCCGT	VCCGT	VCCGT
A68	VCCGT	VCCGT	VCCGT
A69	VCCGT	VCCGT	VCCGT
A70	VCCGT	VCCGT	VCCGT
A71	VCCGT	VCCGT	VCCGT
A72	VCCGT	VCCGT	VCCGT
A73	VCCGT	VCCGT	VCCGT
A74	VCCGT	VCCGT	VCCGT
A75	VCCGT	VCCGT	VCCGT
A76	VCCGT	VCCGT	VCCGT
A77	VCCGT	VCCGT	VCCGT
A78	VCCGT	VCCGT	VCCGT
A79	VCCGT	VCCGT	VCCGT
A80	VCCGT	VCCGT	VCCGT
A81	VCCGT	VCCGT	VCCGT
A82	VCCGT	VCCGT	VCCGT
A83	VCCGT	VCCGT	VCCGT
A84	VCCGT	VCCGT	VCCGT
A85	VCCGT	VCCGT	VCCGT
A86	VCCGT	VCCGT	VCCGT
A87	VCCGT	VCCGT	VCCGT
A88	VCCGT	VCCGT	VCCGT
A89	VCCGT	VCCGT	VCCGT
A90	VCCGT	VCCGT	VCCGT
A91	VCCGT	VCCGT	VCCGT
A92	VCCGT	VCCGT	VCCGT
A93	VCCGT	VCCGT	VCCGT
A94	VCCGT	VCCGT	VCCGT
A95	VCCGT	VCCGT	VCCGT
A96	VCCGT	VCCGT	VCCGT
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A110	VCCGT	VCCGT	VCCGT
A111	VCCGT	VCCGT	VCCGT
A112	VCCGT	VCCGT	VCCGT
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A114	VCCGT	VCCGT	VCCGT
A115	VCCGT	VCCGT	VCCGT
A116	VCCGT	VCCGT	VCCGT
A117	VCCGT	VCCGT	VCCGT
A118	VCCGT	VCCGT	VCCGT
A119	VCCGT	VCCGT	VCCGT
A120	VCCGT	VCCGT	VCCGT
A121	VCCGT	VCCGT	VCCGT
A122	VCCGT	VCCGT	VCCGT
A123	VCCGT	VCCGT	VCCGT
A124	VCCGT	VCCGT	VCCGT
A125	VCCGT	VCCGT	VCCGT
A126	VCCGT	VCCGT	VCCGT
A127	VCCGT	VCCGT	VCCGT
A128	VCCGT	VCCGT	VCCGT
A129	VCCGT	VCCGT	VCCGT
A130	VCCGT	VCCGT	VCCGT
A131	VCCGT	VCCGT	VCCGT
A132	VCCGT	VCCGT	VCCGT
A133	VCCGT	VCCGT	VCCGT
A134	VCCGT	VCCGT	VCCGT
A135	VCCGT	VCCGT	VCCGT
A136	VCCGT	VCCGT	VCCGT
A137	VCCGT	VCCGT	VCCGT
A138	VCCGT	VCCGT	VCCGT
A139	VCCGT	VCCGT	VCCGT
A140	VCCGT	VCCGT	VCCGT
A141	VCCGT	VCCGT	VCCGT
A142	VCCGT	VCCGT	VCCGT
A143	VCCGT	VCCGT	VCCGT
A144	VCCGT	VCCGT	VCCGT
A145	VCCGT	VCCGT	VCCGT
A146	VCCGT	VCCGT	VCCGT
A147	VCCGT	VCCGT	VCCGT
A148	VCCGT	VCCGT	VCCGT
A149	VCCGT	VCCGT	VCCGT
A150	VCCGT	VCCGT	VCCGT
A151	VCCGT	VCCGT	VCCGT
A152	VCCGT	VCCGT	VCCGT
A153	VCCGT	VCCGT	VCCGT
A154	VCCGT	VCCGT	VCCGT
A155	VCCGT	VCCGT	VCCGT
A156	VCCGT	VCCGT	VCCGT
A157	VCCGT	VCCGT	VCCGT
A158	VCCGT	VCCGT	VCCGT
A159	VCCGT	VCCGT	VCCGT
A160	VCCGT	VCCGT	VCCGT
A161	VCCGT	VCCGT	VCCGT
A162	VCCGT	VCCGT	VCCGT
A163	VCCGT	VCCGT	VCCGT
A164	VCCGT	VCCGT	VCCGT
A165	VCCGT	VCCGT	VCCGT
A166	VCCGT	VCCGT	VCCGT
A167	VCCGT	VCCGT	VCCGT
A168	VCCGT	VCCGT	VCCGT
A169	VCCGT	VCCGT	VCCGT
A170	VCCGT	VCCGT	VCCGT
A171	VCCGT	VCCGT	VCCGT
A172	VCCGT	VCCGT	VCCGT
A173	VCCGT	VCCGT	VCCGT
A174	VCCGT	VCCGT	VCCGT
A175	VCCGT	VCCGT	VCCGT
A176	VCCGT	VCCGT	VCCGT
A177	VCCGT	VCCGT	VCCGT
A178	VCCGT	VCCGT	VCCGT
A179	VCCGT	VCCGT	VCCGT
A180	VCCGT	VCCGT	VCCGT
A181	VCCGT	VCCGT	VCCGT
A182	VCCGT	VCCGT	VCCGT
A183	VCCGT	VCCGT	VCCGT
A184	VCCGT	VCCGT	VCCGT
A185	VCCGT	VCCGT	VCCGT
A186	VCCGT	VCCGT	VCCGT
A187	VCCGT	VCCGT	VCCGT
A188	VCCGT	VCCGT	VCCGT
A189	VCCGT	VCCGT	VCCGT
A190	VCCGT	VCCGT	VCCGT
A191	VCCGT	VCCGT	VCCGT
A192	VCCGT	VCCGT	VCCGT
A193	VCCGT	VCCGT	VCCGT
A194	VCCGT	VCCGT	VCCGT
A195	VCCGT	VCCGT	VCCGT
A196	VCCGT	VCCGT	VCCGT
A197	VCCGT	VCCGT	VCCGT
A198	VCCGT	VCCGT	VCCGT
A199	VCCGT	VCCGT	VCCGT
A200	VCCGT	VCCGT	VCCGT

Figure 11-11. Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline

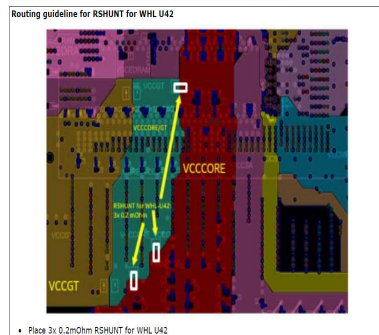
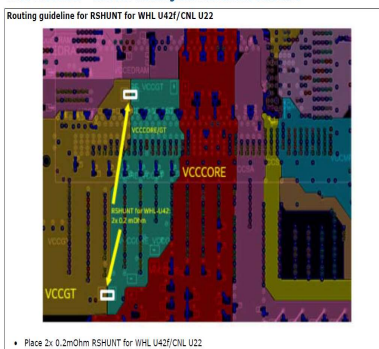


Figure 11-11. Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline



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[illegible]

### 10.3 General DC Characteristics

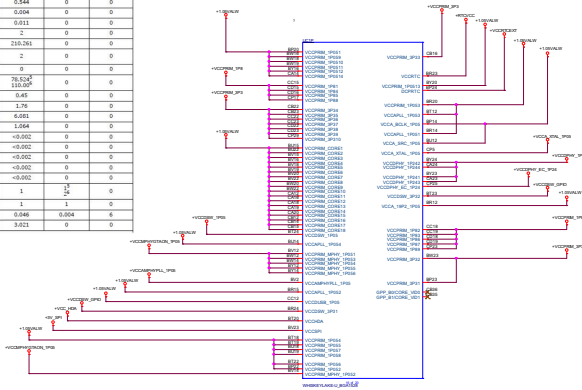
[illegible]

Table 10-9. Other DC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min.	Norm.	Max.	Unit	Notes
VCCCR1_1P05	Core Logic, Ungated SRAM, I/O Blocks, USB APB, Processor Sideband, JTAG, Thermal Sensor, MIP1* DPHY Primary VDDP	0.9975	1.05	1.1025	V	1

88 **Total Confidant**

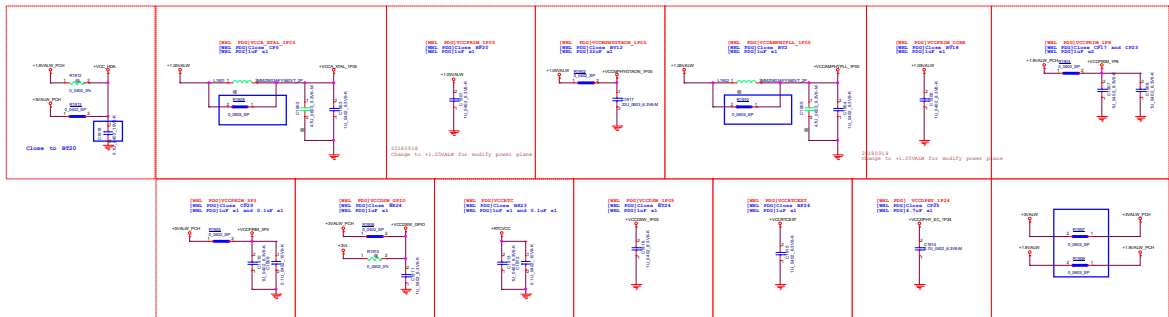
### Electrical Characteristic



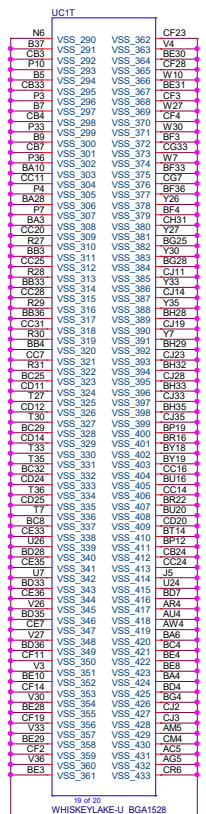
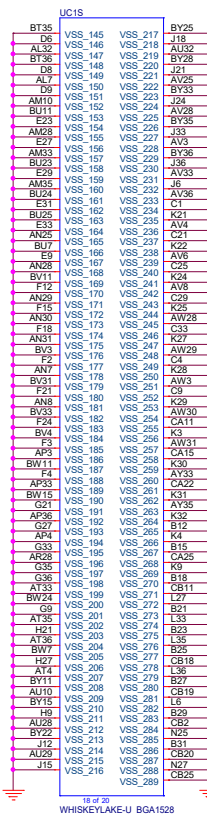
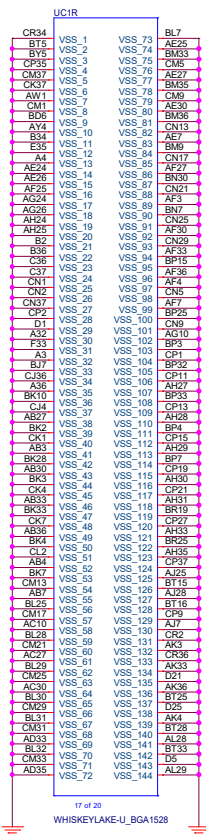
Table 10-9. Other DC Characteristics (Sheet 2 of 2)


Symbol	Parameter	Min.	Max.	Units	Notes
DCPWR1 (1.0V)	1.0V PWR1 PWR1	1.75	1.80	V	1
DCPWR2 (1.0V)	1.0V PWR2 PWR2	1.75	1.80	V	1
DCPWR3 (1.0V)	1.0V PWR3 PWR3	1.75	1.80	V	1
DCPWR4 (1.0V)	1.0V PWR4 PWR4	1.75	1.80	V	1
DCPWR5 (1.0V)	1.0V PWR5 PWR5	1.75	1.80	V	1
DCPWR6 (1.0V)	1.0V PWR6 PWR6	1.75	1.80	V	1
DCPWR7 (1.0V)	1.0V PWR7 PWR7	1.75	1.80	V	1
DCPWR8 (1.0V)	1.0V PWR8 PWR8	1.75	1.80	V	1
DCPWR9 (1.0V)	1.0V PWR9 PWR9	1.75	1.80	V	1
DCPWR10 (1.0V)	1.0V PWR10 PWR10	1.75	1.80	V	1
DCPWR11 (1.0V)	1.0V PWR11 PWR11	1.75	1.80	V	1
DCPWR12 (1.0V)	1.0V PWR12 PWR12	1.75	1.80	V	1
DCPWR13 (1.0V)	1.0V PWR13 PWR13	1.75	1.80	V	1
DCPWR14 (1.0V)	1.0V PWR14 PWR14	1.75	1.80	V	1
DCPWR15 (1.0V)	1.0V PWR15 PWR15	1.75	1.80	V	1
DCPWR16 (1.0V)	1.0V PWR16 PWR16	1.75	1.80	V	1
DCPWR17 (1.0V)	1.0V PWR17 PWR17	1.75	1.80	V	1
DCPWR18 (1.0V)	1.0V PWR18 PWR18	1.75	1.80	V	1
DCPWR19 (1.0V)	1.0V PWR19 PWR19	1.75	1.80	V	1
DCPWR20 (1.0V)	1.0V PWR20 PWR20	1.75	1.80	V	1
DCPWR21 (1.0V)	1.0V PWR21 PWR21	1.75	1.80	V	1
DCPWR22 (1.0V)	1.0V PWR22 PWR22	1.75	1.80	V	1
DCPWR23 (1.0V)	1.0V PWR23 PWR23	1.75	1.80	V	1
DCPWR24 (1.0V)	1.0V PWR24 PWR24	1.75	1.80	V	1
DCPWR25 (1.0V)	1.0V PWR25 PWR25	1.75	1.80	V	1
DCPWR26 (1.0V)	1.0V PWR26 PWR26	1.75	1.80	V	1
DCPWR27 (1.0V)	1.0V PWR27 PWR27	1.75	1.80	V	1
DCPWR28 (1.0V)	1.0V PWR28 PWR28	1.75	1.80	V	1
DCPWR29 (1.0V)	1.0V PWR29 PWR29	1.75	1.80	V	1
DCPWR30 (1.0V)	1.0V PWR30 PWR30	1.75	1.80	V	1
DCPWR31 (1.0V)	1.0V PWR31 PWR31	1.75	1.80	V	1
DCPWR32 (1.0V)	1.0V PWR32 PWR32	1.75	1.80	V	1
DCPWR33 (1.0V)	1.0V PWR33 PWR33	1.75	1.80	V	1
DCPWR34 (1.0V)	1.0V PWR34 PWR34	1.75	1.80	V	1
DCPWR35 (1.0V)	1.0V PWR35 PWR35	1.75	1.80	V	1
DCPWR36 (1.0V)	1.0V PWR36 PWR36	1.75	1.80	V	1
DCPWR37 (1.0V)	1.0V PWR37 PWR37	1.75	1.80	V	1
DCPWR38 (1.0V)	1.0V PWR38 PWR38	1.75	1.80	V	1
DCPWR39 (1.0V)	1.0V PWR39 PWR39	1.75	1.80	V	1
DCPWR40 (1.0V)	1.0V PWR40 PWR40	1.75	1.80	V	1
DCPWR41 (1.0V)	1.0V PWR41 PWR41	1.75	1.80	V	1
DCPWR42 (1.0V)	1.0V PWR42 PWR42	1.75	1.80	V	1
DCPWR43 (1.0V)	1.0V PWR43 PWR43	1.75	1.80	V	1
DCPWR44 (1.0V)	1.0V PWR44 PWR44	1.75	1.80	V	1
DCPWR45 (1.0V)	1.0V PWR45 PWR45	1.75	1.80	V	1
DCPWR46 (1.0V)	1.0V PWR46 PWR46	1.75	1.80	V	1
DCPWR47 (1.0V)	1.0V PWR47 PWR47	1.75	1.80	V	1
DCPWR48 (1.0V)	1.0V PWR48 PWR48	1.75	1.80	V	1
DCPWR49 (1.0V)	1.0V PWR49 PWR49	1.75	1.80	V	1
DCPWR50 (1.0V)	1.0V PWR50 PWR50	1.75	1.80	V	1
DCPWR51 (1.0V)	1.0V PWR51 PWR51	1.75	1.80	V	1
DCPWR52 (1.0V)	1.0V PWR52 PWR52	1.75	1.80	V	1
DCPWR53 (1.0V)	1.0V PWR53 PWR53	1.75	1.80	V	1
DCPWR54 (1.0V)	1.0V PWR54 PWR54	1.75	1.80	V	1
DCPWR55 (1.0V)	1.0V PWR55 PWR55	1.75	1.80	V	1
DCPWR56 (1.0V)	1.0V PWR56 PWR56	1.75	1.80	V	1
DCPWR57 (1.0V)	1.0V PWR57 PWR57	1.75	1.80	V	1
DCPWR58 (1.0V)	1.0V PWR58 PWR58	1.75	1.80	V	1
DCPWR59 (1.0V)	1.0V PWR59 PWR59	1.75	1.80	V	1
DCPWR60 (1.0V)	1.0V PWR60 PWR60	1.75	1.80	V	1
DCPWR61 (1.0V)	1.0V PWR61 PWR61	1.75	1.80	V	1
DCPWR62 (1.0V)	1.0V PWR62 PWR62	1.75	1.80	V	1
DCPWR63 (1.0V)	1.0V PWR63 PWR63	1.75	1.80	V	1
DCPWR64 (1.0V)	1.0V PWR64 PWR64	1.75	1.80	V	1
DCPWR65 (1.0V)	1.0V PWR65 PWR65	1.75	1.80	V	1
DCPWR66 (1.0V)	1.0V PWR66 PWR66	1.75	1.80	V	1
DCPWR67 (1.0V)	1.0V PWR67 PWR67	1.75	1.80	V	1
DCPWR68 (1.0V)	1.0V PWR68 PWR68	1.75	1.80	V	1
DCPWR69 (1.0V)	1.0V PWR69 PWR69	1.75	1.80	V	1
DCPWR70 (1.0V)	1.0V PWR70 PWR70	1.75	1.80	V	1
DCPWR71 (1.0V)	1.0V PWR71 PWR71	1.75	1.80	V	1
DCPWR72 (1.0V)	1.0V PWR72 PWR72	1.75	1.80	V	1
DCPWR73 (1.0V)	1.0V PWR73 PWR73	1.75	1.80	V	1
DCPWR74 (1.0V)	1.0V PWR74 PWR74	1.75	1.80	V	1
DCPWR75 (1.0V)	1.0V PWR75 PWR75	1.75	1.80	V	1
DCPWR76 (1.0V)	1.0V PWR76 PWR76	1.75	1.80	V	1
DCPWR77 (1.0V)	1.0V PWR77 PWR77	1.75	1.80	V	1
DCPWR78 (1.0V)	1.0V PWR78 PWR78	1.75	1.80	V	1
DCPWR79 (1.0V)	1.0V PWR79 PWR79	1.75	1.80	V	1
DCPWR80 (1.0V)	1.0V PWR80 PWR80	1.75	1.80	V	1
DCPWR81 (1.0V)	1.0V PWR81 PWR81	1.75	1.80	V	1
DCPWR82 (1.0V)	1.0V PWR82 PWR82	1.75	1.80	V	1
DCPWR83 (1.0V)	1.0V PWR83 PWR83	1.75	1.80	V	1
DCPWR84 (1.0V)	1.0V PWR84 PWR84	1.75	1.80	V	1
DCPWR85 (1.0V)	1.0V PWR85 PWR85	1.75	1.80	V	1
DCPWR86 (1.0V)	1.0V PWR86 PWR86	1.75	1.80	V	1
DCPWR87 (1.0V)	1.0V PWR87 PWR87	1.75	1.80	V	1
DCPWR88 (1.0V)	1.0V PWR88 PWR88	1.75	1.80	V	1
DCPWR89 (1.0V)	1.0V PWR89 PWR89	1.75	1.80	V	1
DCPWR90 (1.0V)	1.0V PWR90 PWR90	1.75	1.80	V	1
DCPWR91 (1.0V)	1.0V PWR91 PWR91	1.75	1.80	V	1
DCPWR92 (1.0V)	1.0V PWR92 PWR92	1.75	1.80	V	1
DCPWR93 (1.0V)	1.0V PWR93 PWR93	1.75	1.80	V	1
DCPWR94 (1.0V)	1.0V PWR94 PWR94	1.75	1.80	V	1
DCPWR95 (1.0V)	1.0V PWR95 PWR95	1.75	1.80	V	1
DCPWR96 (1.0V)	1.0V PWR96 PWR96	1.75	1.80	V	1
DCPWR97 (1.0V)	1.0V PWR97 PWR97	1.75	1.80	V	1
DCPWR98 (1.0V)	1.0V PWR98 PWR98	1.75	1.80	V	1
DCPWR99 (1.0V)	1.0V PWR99 PWR99	1.75	1.80	V	1
DCPWR100 (1.0V)	1.0V PWR100 PWR100	1.75	1.80	V	1
DCPWR101 (1.0V)	1.0V PWR101 PWR101	1.75	1.80	V	1
DCPWR102 (1.0V)	1.0V PWR102 PWR102	1.75	1.80	V	1
DCPWR103 (1.0V)	1.0V PWR103 PWR103	1.75	1.80	V	1
DCPWR104 (1.0V)	1.0V PWR104 PWR104	1.75	1.80	V	1
DCPWR105 (1.0V)	1.0V PWR105 PWR105	1.75	1.80	V	1
DCPWR106 (1.0V)	1.0V PWR106 PWR106	1.75	1.80	V	1
DCPWR107 (1.0V)	1.0V PWR107 PWR107	1.75	1.80	V	1
DCPWR108 (1.0V)	1.0V PWR108 PWR108	1.75	1.80	V	1
DCPWR109 (1.0V)	1.0V PWR109 PWR109	1.75	1.80	V	1
DCPWR110 (1.0V)	1.0V PWR110 PWR110	1.75	1.80	V	1
DCPWR111 (1.0V)	1.0V PWR111 PWR111	1.75	1.80	V	1
DCPWR112 (1.0V)	1.0V PWR112 PWR112	1.75	1.80	V	1
DCPWR113 (1.0V)	1.0V PWR113 PWR113	1.75	1.80	V	1
DCPWR114 (1.0V)	1.0V PWR114 PWR114	1.75	1.80	V	1
DCPWR115 (1.0V)	1.0V PWR115 PWR115	1.75	1.80	V	1
DCPWR116 (1.0V)	1.0V PWR116 PWR116	1.75	1.80	V	1
DCPWR117 (1.0V)	1.0V PWR117 PWR117	1.75	1.80	V	1
DCPWR118 (1.0V)	1.0V PWR118 PWR118	1.75	1.80	V	1
DCPWR119 (1.0V)	1.0V PWR119 PWR119	1.75	1.80	V	1
DCPWR120 (1.0V)	1.0V PWR120 PWR120	1.75	1.80	V	1
DCPWR121 (1.0V)	1.0V PWR121 PWR121	1.75	1.80	V	1
DCPWR122 (1.0V)	1.0V PWR122 PWR122	1.75	1.80	V	1
DCPWR123 (1.0V)	1.0V PWR123 PWR123	1.75	1.80	V	1
DCPWR124 (1.0V)	1.0V PWR124 PWR124	1.75	1.80	V	1
DCPWR125 (1.0V)	1.0V PWR125 PWR125	1.75	1.80	V	1
DCPWR126 (1.0V)	1.0V PWR126 PWR126	1.75	1.80	V	1
DCPWR127 (1.0V)	1.0V PWR127 PWR127	1.75	1.80	V	1
DCPWR128 (1.0V)	1.0V PWR128 PWR128	1.75	1.80	V	1
DCPWR129 (1.0V)	1.0V PWR129 PWR129	1.75	1.80	V	1
DCPWR130 (1.0V)	1.0V PWR130 PWR130	1.75	1.80	V	1
DCPWR131 (1.0V)	1.0V PWR131 PWR131	1.75	1.80	V	1
DCPWR132 (1.0V)	1.0V PWR132 PWR132	1.75	1.80	V	1
DCPWR133 (1.0V)	1.0V PWR133 PWR133	1.75	1.80	V	1
DCPWR134 (1.0V)	1.0V PWR134 PWR134	1.75	1.80	V	1
DCPWR135 (1.0V)	1.0V PWR135 PWR135	1.75	1.80	V	1
DCPWR136 (1.0V)	1.0V PWR136 PWR136	1.75	1.80	V	1
DCPWR137 (1.0V)	1.0V PWR137 PWR137	1.75	1.80	V	1
DCPWR138 (1.0V)	1.0V PWR138 PWR138	1.75	1.80	V	1
DCPWR139 (1.0V)	1.0V PWR139 PWR139	1.75	1.80	V	1
DCPWR140 (1.0V)	1.0V PWR140 PWR140	1.75	1.80	V	1
DCPWR141 (1.0V)	1.0V PWR141 PWR141	1.75	1.80	V	1
DCPWR142 (1.0V)	1.0V PWR142 PWR142	1.75	1.80	V	1
DCPWR143 (1.0V)	1.0V PWR143 PWR143	1.75	1.80	V	1
DCPWR144 (1.0V)	1.0V PWR144 PWR144	1.75	1.80	V	1
DCPWR145 (1.0V)	1.0V PWR145 PWR145	1.75	1.80	V	1
DCPWR146 (1.0V)	1.0V PWR146 PWR146	1.75	1.80	V	1
DCPWR147 (1.0V)	1.0V PWR147 PWR147	1.75	1.80	V	1
DCPWR148 (1.0V)	1.0V PWR148 PWR148	1.75	1.80	V	1
DCPWR149 (1.0V)	1.0V PWR149 PWR149	1.75	1.80	V	1
DCPWR150 (1.0V)	1.0V PWR150 PWR150	1.75	1.80	V	1
DCPWR151 (1.0V)	1.0V PWR151 PWR151	1.75	1.80	V	1
DCPWR152 (1.0V)	1.0V PWR152 PWR152	1.75	1.80	V	1
DCPWR153 (1.0V)	1.0V PWR153 PWR153	1.75	1.80	V	1
DCPWR154 (1.0V)	1.0V PWR154 PWR154	1.75	1.80	V	1
DCPWR155 (1.0V)	1.0V PWR155 PWR155	1.75	1.80	V	1
DCPWR156 (1.0V)	1.0V PWR156 PWR156	1.75	1.80	V	1
DCPWR157 (1.0V)	1.0V PWR157 PWR157	1.75	1.80	V	1
DCPWR158 (1.0V)	1.0V PWR158 PWR158	1.75	1.80	V	1
DCPWR159 (1.0V)	1.0V PWR159 PWR159	1.75	1.80	V	1
DCPWR160 (1.0V)	1.0V PWR160 PWR160	1.75	1.80	V	1
DCPWR161 (1.0V)	1.0V PWR161 PWR161	1.75	1.80	V	1
DCPWR162 (1.0V)	1.0V PWR162 PWR162	1.75	1.80	V	1
DCPWR163 (1.0V)	1.0V PWR163 PWR163	1.75	1.80	V	1
DCPWR164 (1.0V)	1.0V PWR164 PWR164	1.75	1.80	V	1
DCPWR165 (1.0V)	1.0V PWR165 PWR165	1.75	1.80	V	1
DCPWR166 (1.0V)	1.0V PWR166 PWR166	1.75	1.80	V	1
DCPWR167 (1.0V)	1.0V PWR167 PWR167	1.75	1.80	V	1
DCPWR168 (1.0V)	1.0V PWR168 PWR168	1.75	1.80	V	1
DCPWR169 (1.0V)	1.0V PWR169 PWR169	1.75	1.80	V	1
DCPWR170 (1.0V)	1.0V PWR170 PWR170	1.75	1.80	V	1
DCPWR171 (1.0V)	1.0V PWR171 PWR171	1.75	1.80	V	1
DCPWR172 (1.0V)	1.0V PWR172 PWR172	1.75	1.80	V	1
DCPWR173 (1.0V)	1.0V PWR173 PWR173	1.75	1.80	V	1
DCPWR174 (1.0V)	1.0V PWR174 PWR174	1.75	1.80	V	1
DCPWR175 (1.0V)	1.0V PWR175 PWR175	1.75	1.80	V	1
DCPWR176 (1.0V)	1.0V PWR176 PWR176	1.75	1.80	V	1
DCPWR177 (1.0V)	1.0V PWR177 PWR177	1.75	1.80	V	1
DCPWR178 (1.0V)	1.0V PWR178 PWR178	1.75	1.80	V	1
DCPWR179 (1.0V)	1.0V PWR179 PWR179	1.75	1.80	V	1
DCPWR180 (1.0V)	1.0V PWR180 PWR180	1.75	1.80	V	1
DCPWR181 (1.0V)	1.0V PWR181 PWR181	1.75	1.80	V	1
DCPWR182 (1.0V)	1.0V PWR182 PWR182	1.75	1.80	V	1
DCPWR183 (1.0V)	1.0V PWR183 PWR183	1.75	1.80	V	1
DCPWR184 (1.0V)	1.0V PWR184 PWR184	1.75	1.80	V	1
DCPWR185 (1.0V)	1.0V PWR185 PWR185	1.75	1.80	V	1
DCPWR186 (1.0V)	1.0V PWR186 PWR186	1.75	1.80	V	1
DCPWR187 (1.0V)					

1. The I/O buffer supply voltage is measured at the PCH package pins. The tolerances shown in Table 33-3, "Other DC Characteristics" are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a roll off of 30dB/decade above 20 MHz.
2. Maximum Crystal FSR is 50 ppm.

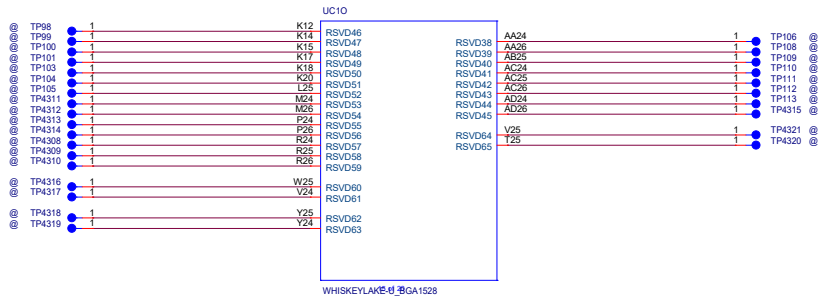



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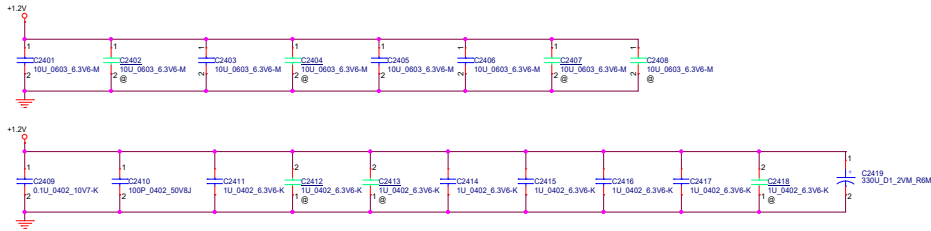
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+2.5V  
+1.2V  
+0.6V

[WHL PDG]VDDQ  
[WHL PDG] EE 10uF x16, 1uF x16. 330uF x1  
Place 10uF/1uF decoupling cap, 4  
near each side of the DIMM  
connector close to VDD pins.  
330uF placeholder

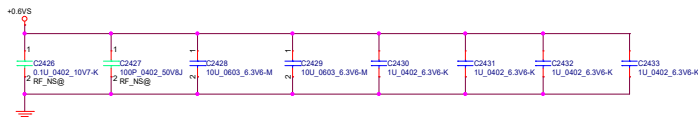
Total quantity is referring to 2 channels.



[WHL PDG]VPP  
[WHL PDG] EE 10uF x2, 1uF x2.  
Place decoupling cap on DRAM side.



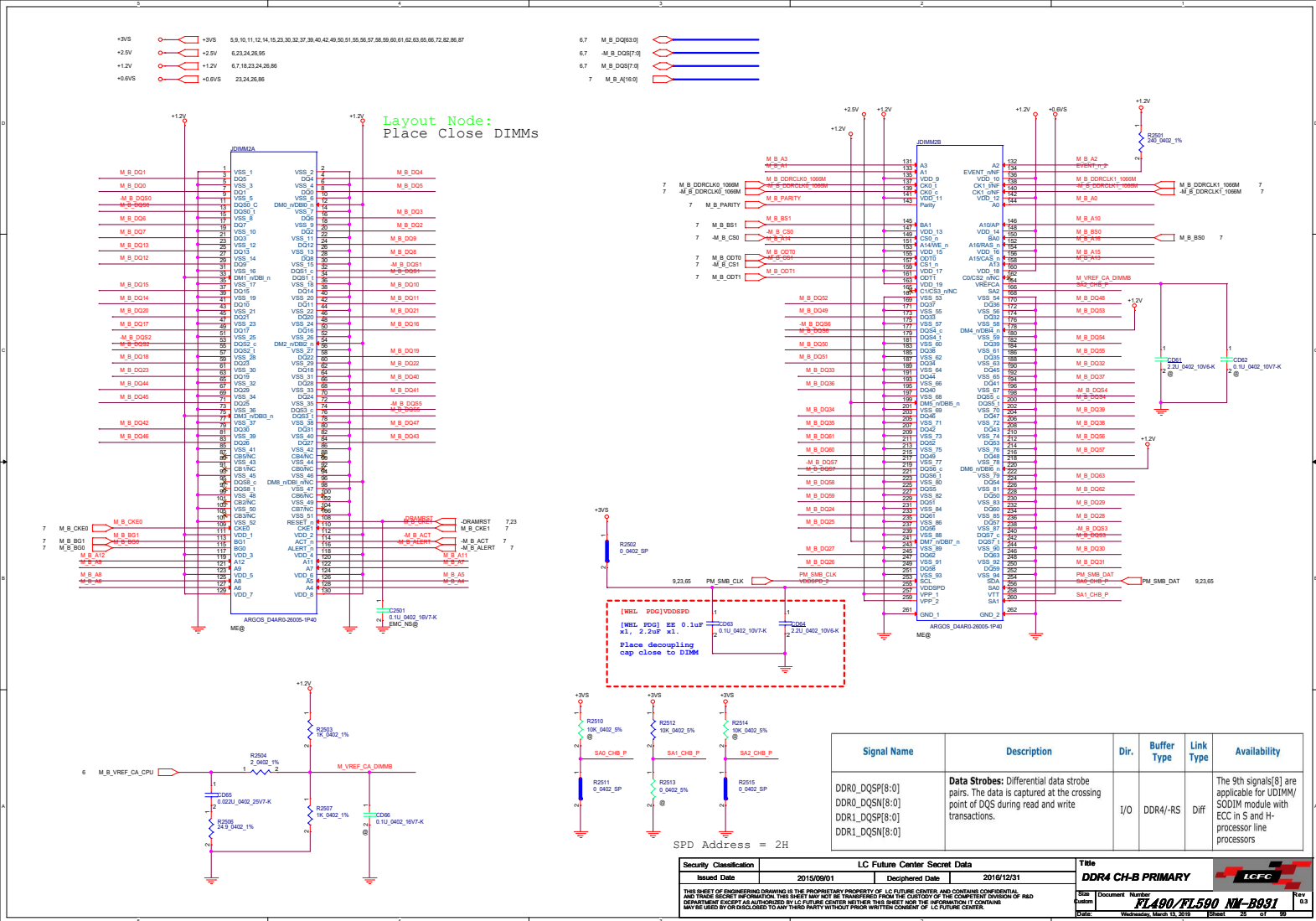
[WHL PDG]VTT  
[WHL PDG] EE 10uF x2, 1uF x4.



Place decoupling on the VTT plane close to SODIMM

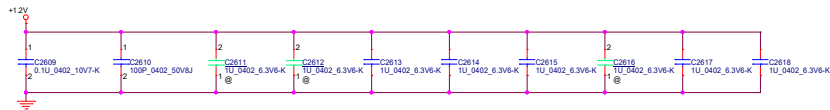
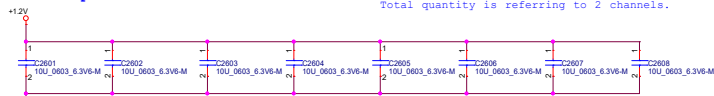
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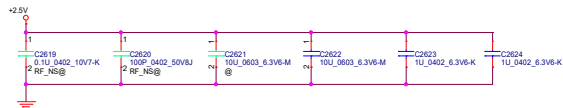


+2.5V  
+1.2V  
+0.6VS

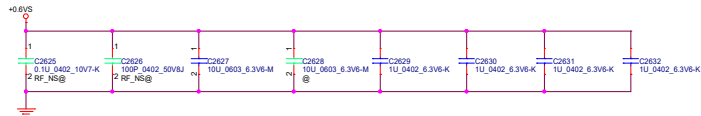
[WHL PDG]VDDQ  
[WHL PDG] EE 10uF x16, 1uF x16. 330uF x1  
Place 10uF/1uF decoupling cap, 4  
near each side of the DIMM  
connector close to VDD pins.  
330uF placeholder  
Total quantity is referring to 2 channels.



[WHL PDG]VPP  
[WHL PDG] EE 10uF x2, 1uF x2.  
Place decoupling cap on DRAM side.

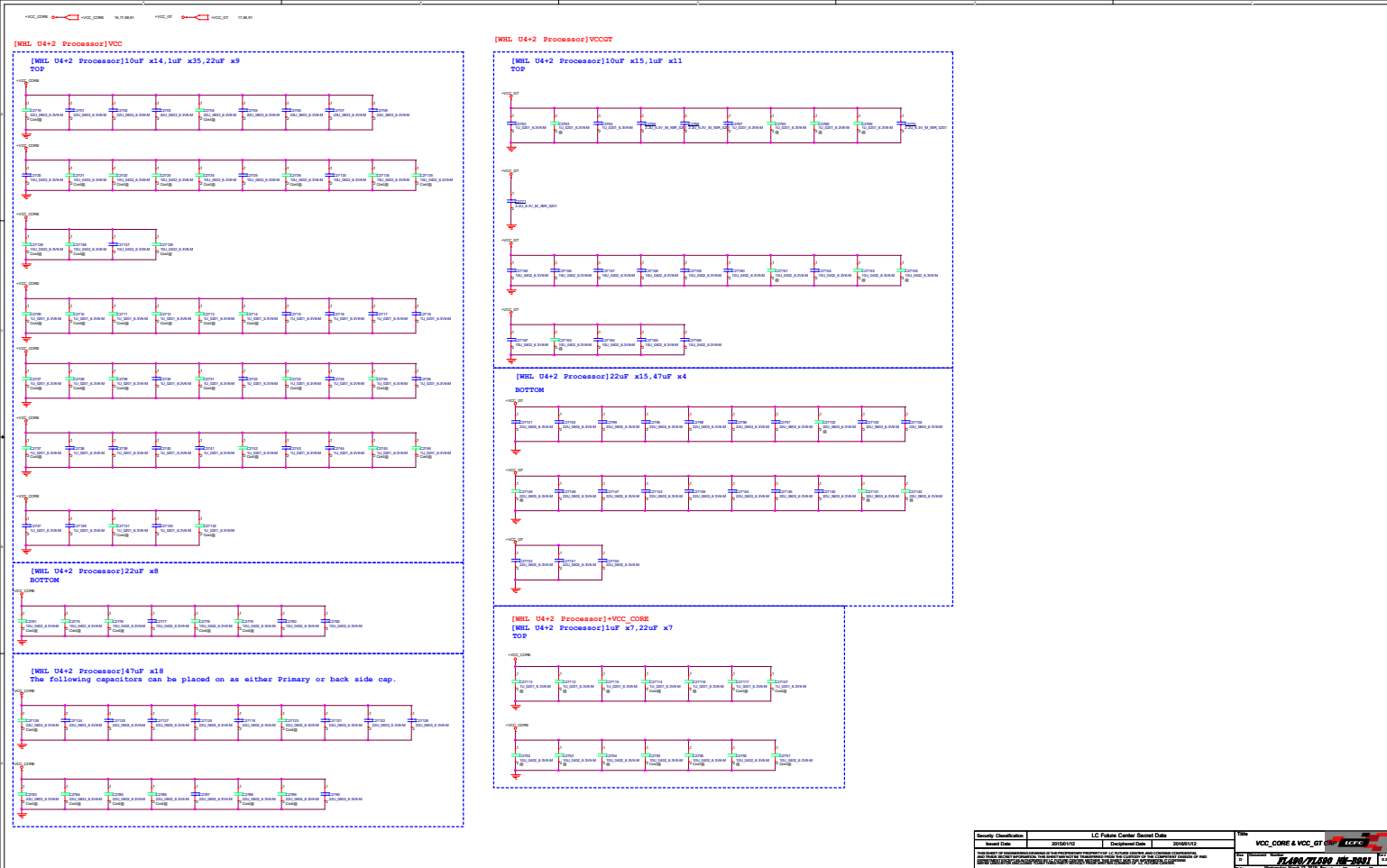


[WHL PDG]VTT  
[WHL PDG] EE 10uF x2, 1uF x4.

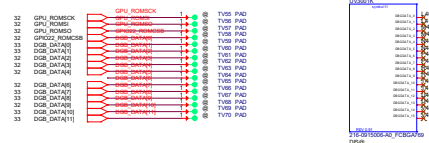


Place decoupling on the VTT plane close to SODIMM

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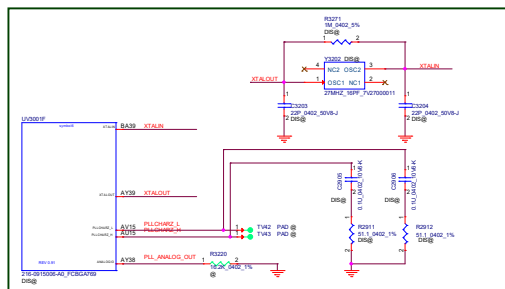
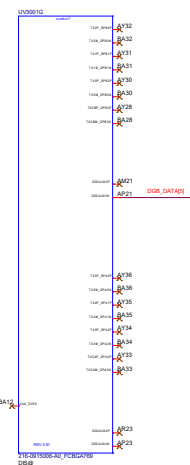


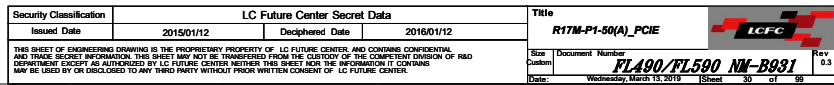
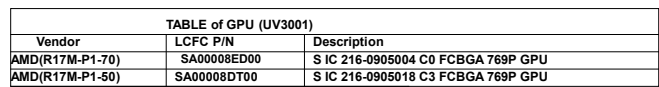


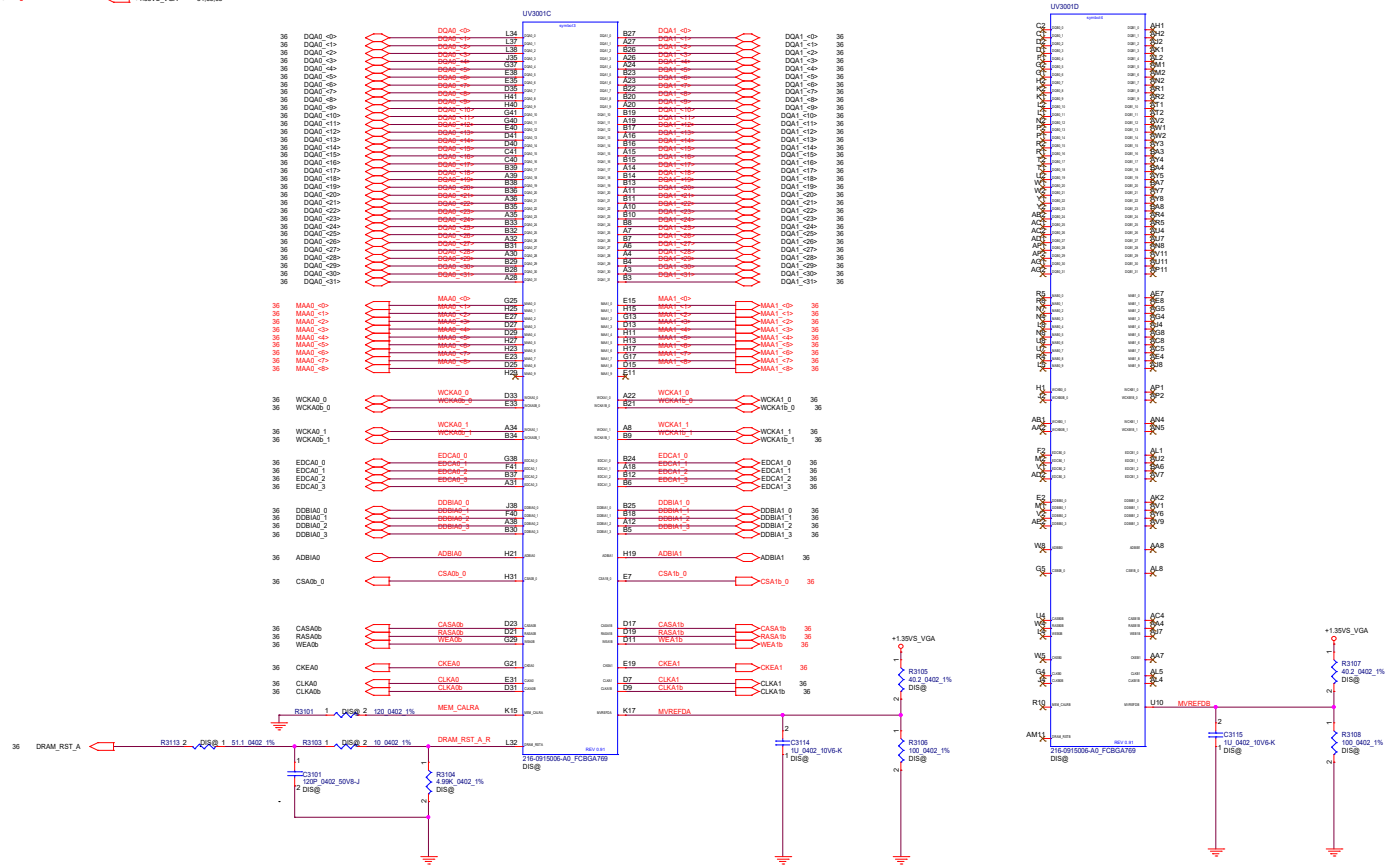



MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	1
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	PS_3[3:1] 01 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

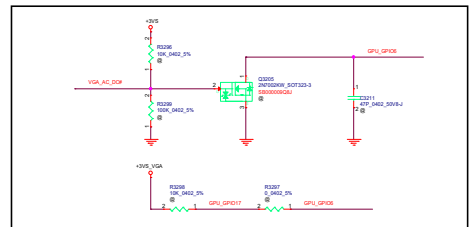
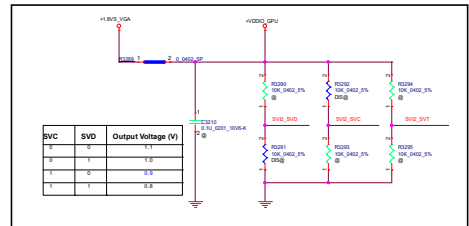
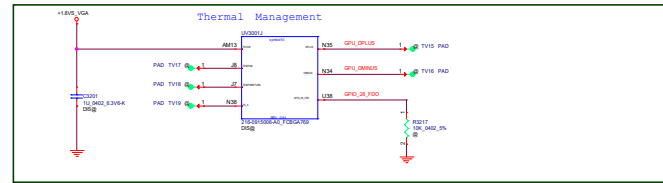
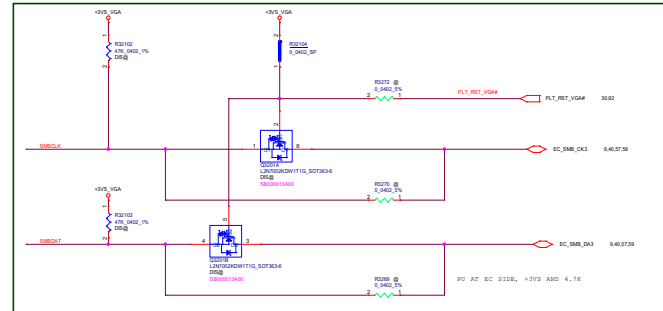
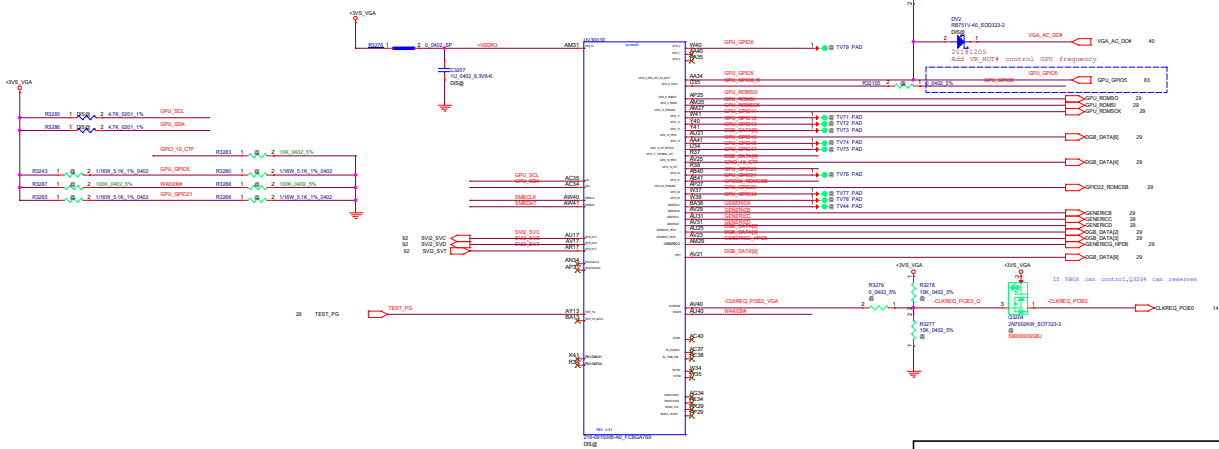







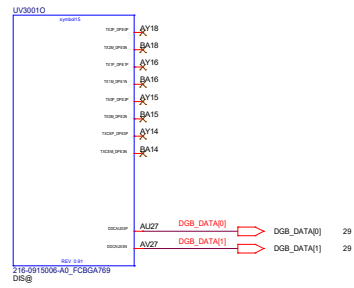
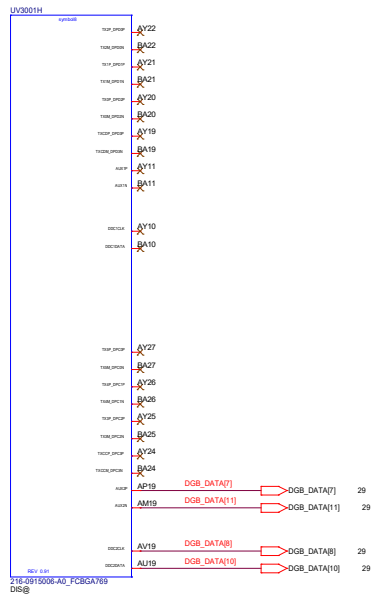
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+1.8V\_VGA 20.3034,3832  
 +0V 0.0  
 +3.0V\_VGA 30.2738,3832



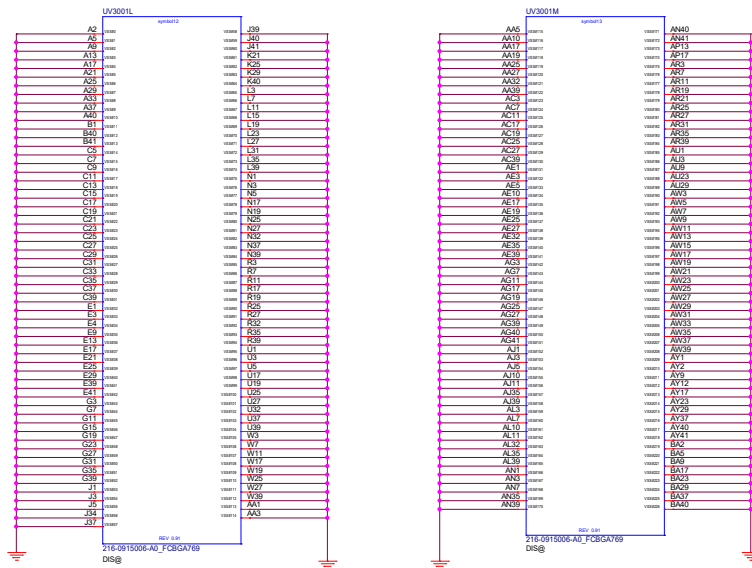
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Code	Washington March 1952		Code	NM 32	





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Revision		Document Number		Rev	
Date		Wednesday, March 11, 2015		Sheet 33 of 39	





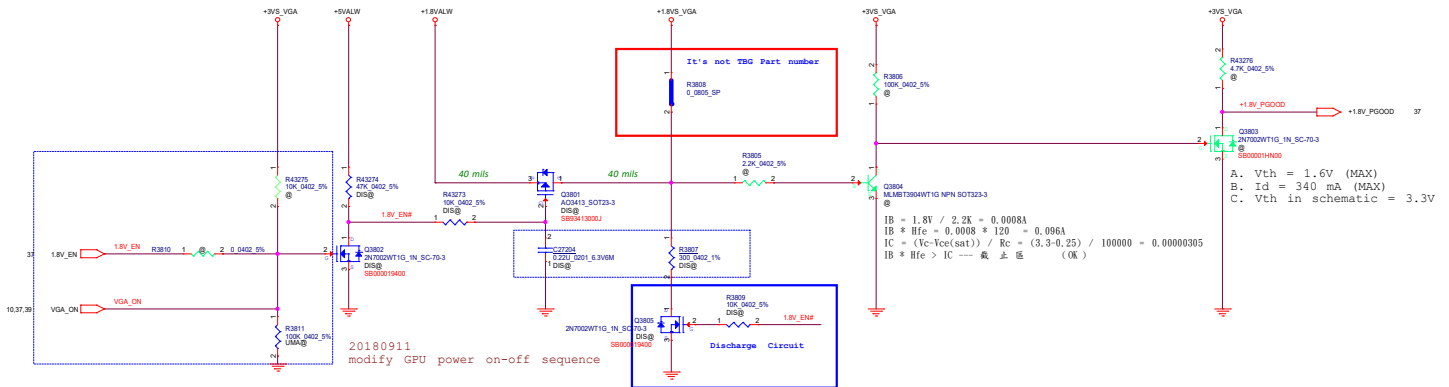
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				Date	Wednesday, March 18, 2015 Sheet 35 of 99

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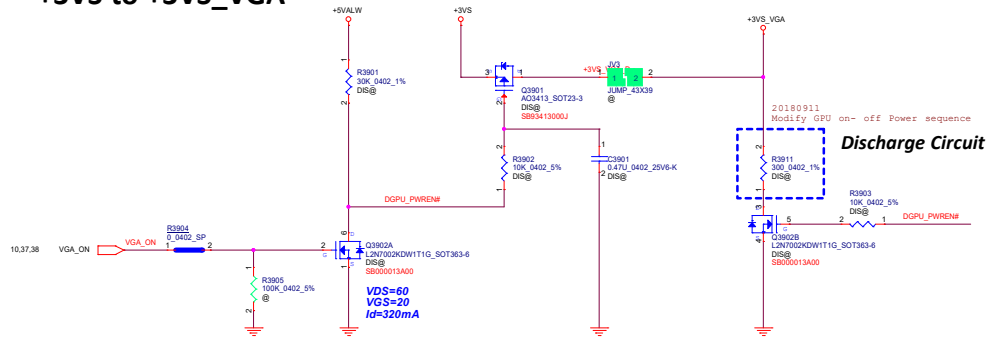


# +1.8VALW to +1.8VS\_VGA

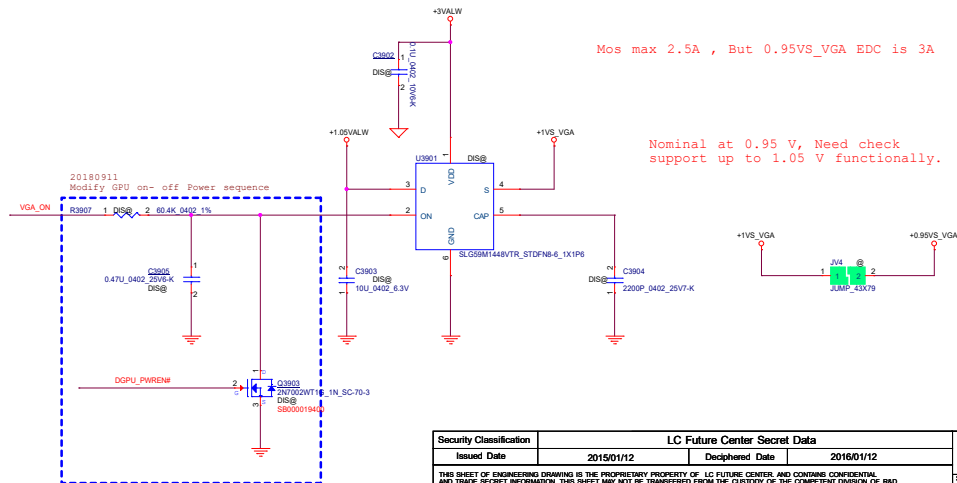


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Issued Date	2015/01/12	Deciphered Date	2016/01/12	R17M-M1-70_PW SWITCH	
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Cust		Document Number		Rev	
Date		Version		0.3	
		FL490/FL590 NM-B931			
		1.3			
		Wednesday, March 25, 2016		Sheet 1 of 1	

## +3VS to +3VS\_VGA



## +1VALW to +1VS\_VGA



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Title	
R17M-M1-70_PW SWITCH	
Size	Document Number
Customer	FL490/FL590 NM-B891
Date	Wednesday, March 15, 2015
Sheet	35 of 99
Rev	0.3





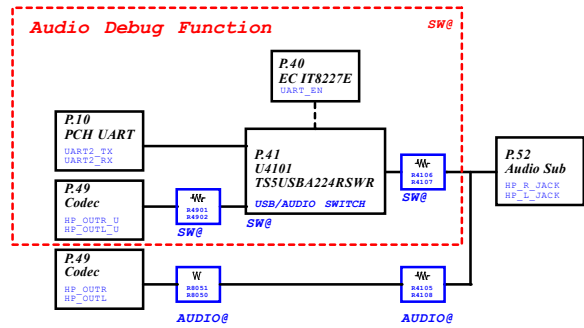
## LAYOUT/ROUTING GUIDELINES

1. For the ADC layout notice circuits,  
a) Keep the trace away from Power, fast data bus, and CRTs. Especially PWM DC-DC control.  
b) Isolate Analog and Digital ground plane.

2. For all power plane,

- a) For the VSTBY circuits,  
\*Recommended net "VSTBY" minimum trace width 12mils.
- b) For the VBAT circuits,  
1) Vbat should be routed with a minimum trace width of 12 mils.  
2) Please make the trace length short, and the trace width wide enough.  
3) Isolate the pin-Vbat of EC and the pin of south bridge VCCRTC to avoid VBAT drops.  
4) The capacitor connected to Diode is spare for battery installation glitch.
- c) For the PLL power circuits,  
Internal PLL is supplied by power pin127 of EC only and may have some filter circuit.

3. For SPI clock lines,  
a) If possible, please avoid using any through-hole.  
b) Do not use multiple signal layers for clock signals.  
c) Please make the trace length short, and the trace width wide enough.  
EC should close to PCH for HSPI signals & SPI flash should close to EC for FSPI signals.  
d) The spacing to the closest neighbor should be wide enough.  
e) The discrete damping resistors and capacitors are recommended.  
f) Keep clock traces as straight as possible. Use arc-shaped traces instead of right-angle bends.



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SCDS306 - OCTOBER 2010

FUNCTION TABLE

A_SEL	V_AUDIO	V_BUS	L_R	D+, D-
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF <sup>(1)</sup>	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

(1) 100Ω shunt resistors are enabled in this state.

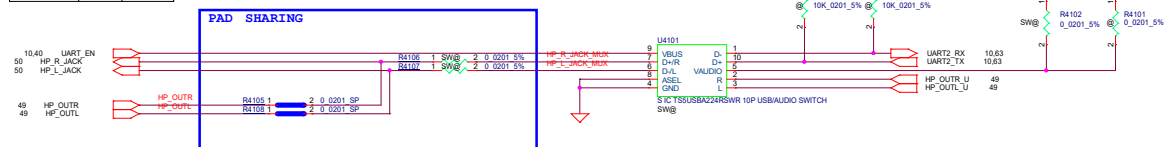
## AUDIO DEBUG PORT

TABLE:

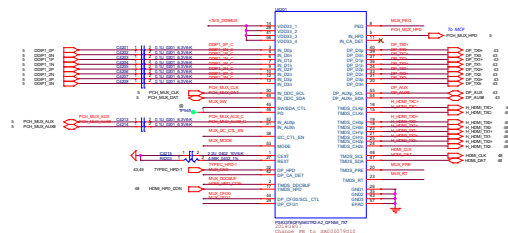
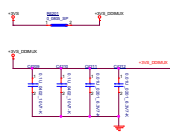
Part Name	For NPI	For MP
U4101 SW@	ASM	NA
R4102 SW@	ASM	NA
R4106 SW@	ASM	NA
R4107 SW@	ASM	NA
R5014 SW@	ASM	NA
R5015 SW@	ASM	NA
R4105 AUDIO@	NA	ASM
R4108 AUDIO@	NA	ASM

TABLE:

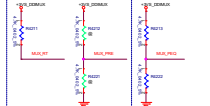
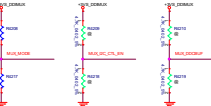
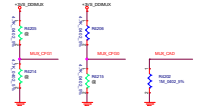
Mode	Audio	UART
UART_EN	L	H



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Quantity	FL490/FL590 NM-B891	Date	Wednesday, March 15, 2015
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# Auto Mode DP Highest Priority



# Pass Through Mode

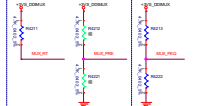


TABLE: Automatic Switching Mode (MODE=H or W)	
SWITCH_PRIORITY	
L: DP Port has higher priority when both ports are plugged	← DEFAULT
H: TMS Port has higher priority when both ports are plugged	
MODE =	
H: Automatic Switching mode, ID Enabled	
W: Automatic Switching mode, ID Disabled	← DEFAULT
L: Control Switching mode, ID Disabled	

20140110  
1. Change SW1 SW2 to SW1, changing priority control by SW1  
2. Add SW1 to SW2 and SW2 to SW1

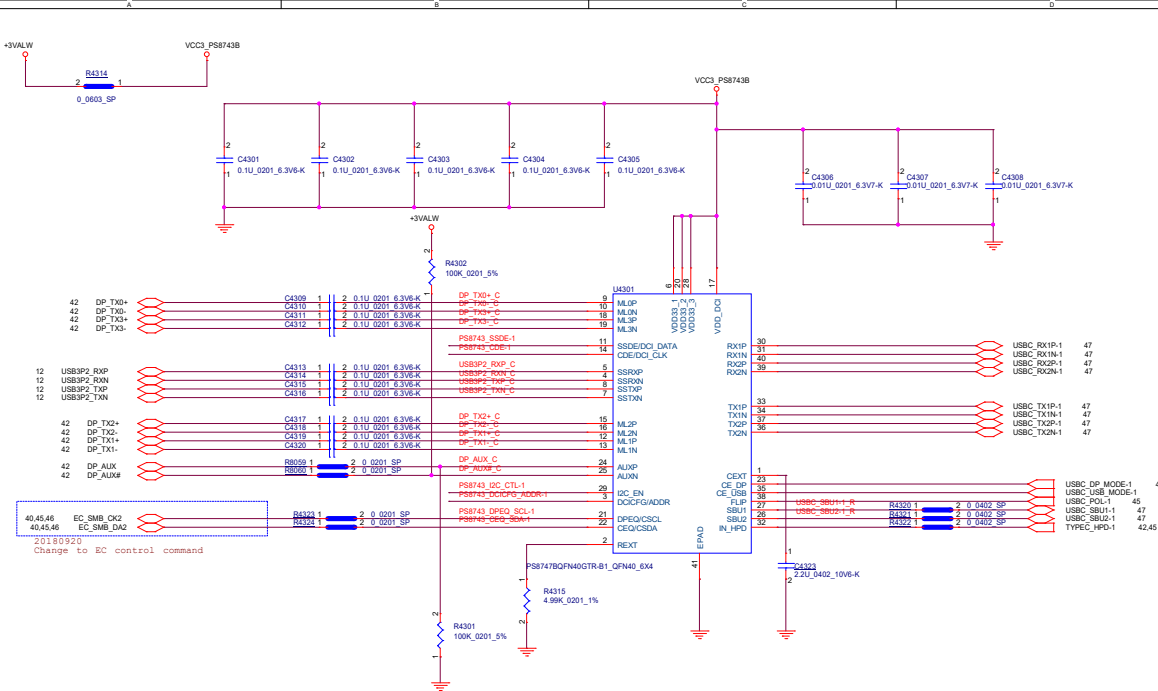
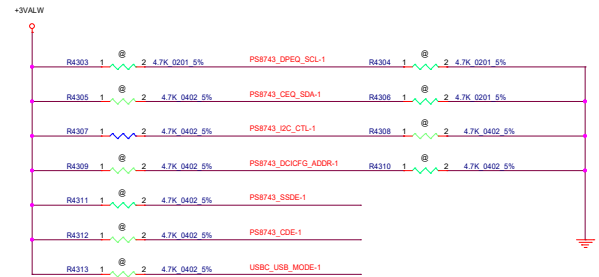
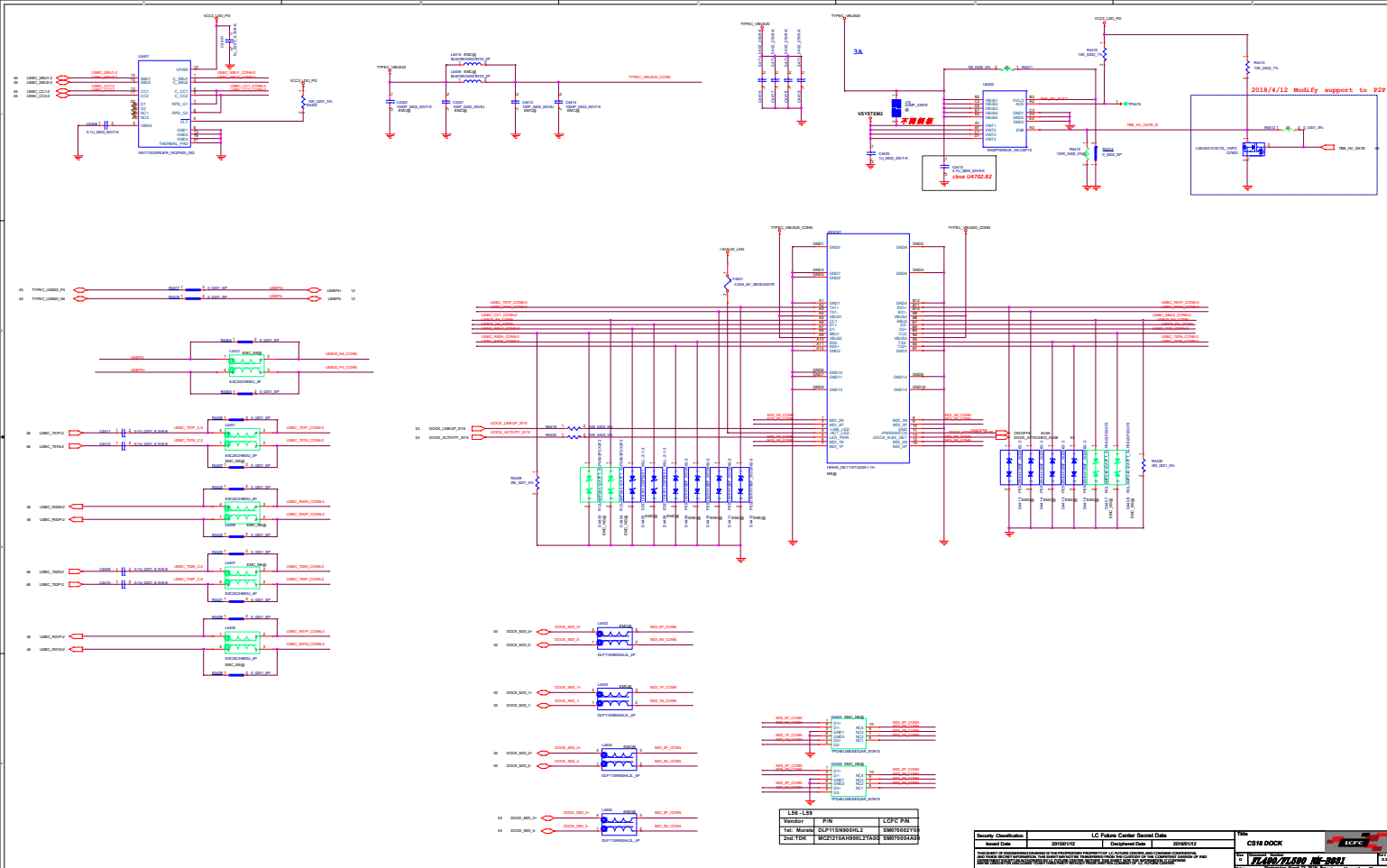


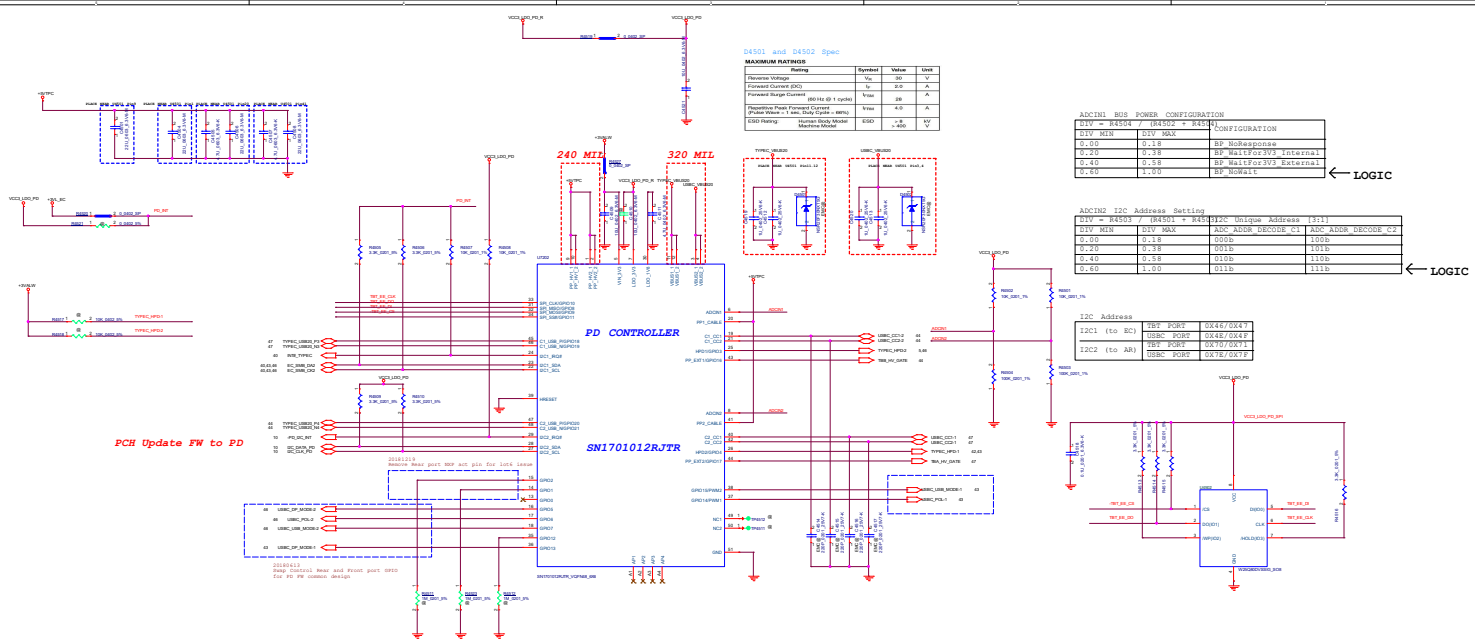
TABLE:

Module Configuration for PS8743 Mode Selection				
State #	CE DP Pin23 (CTL1)	CE USB Pin35 (CTL0)	FLIP Pin38 (FLIP)	MODE
0	H	H	H	1-port USB on SS2 2-lane DP . DP ML0 is on SSRX1(Flipped)
1	H	H	L	1-port USB on SS1 2-lane DP . DP ML0 is on SSRX2(Un-flipped)
2	H	L	H	4-lane DP . DP ML0 is on SSRX1(Flipped)
3	H	L	L	4-lane DP . DP ML0 is on SSRX2(Un-flipped)
4	L	H	H	1-port USB only on SS2 channels (Flipped)
5	L	H	L	1-port USB only on SS1 channels (Un-flipped)
6	L	L	H	Chip power down
7	L	L	L	Chip power down



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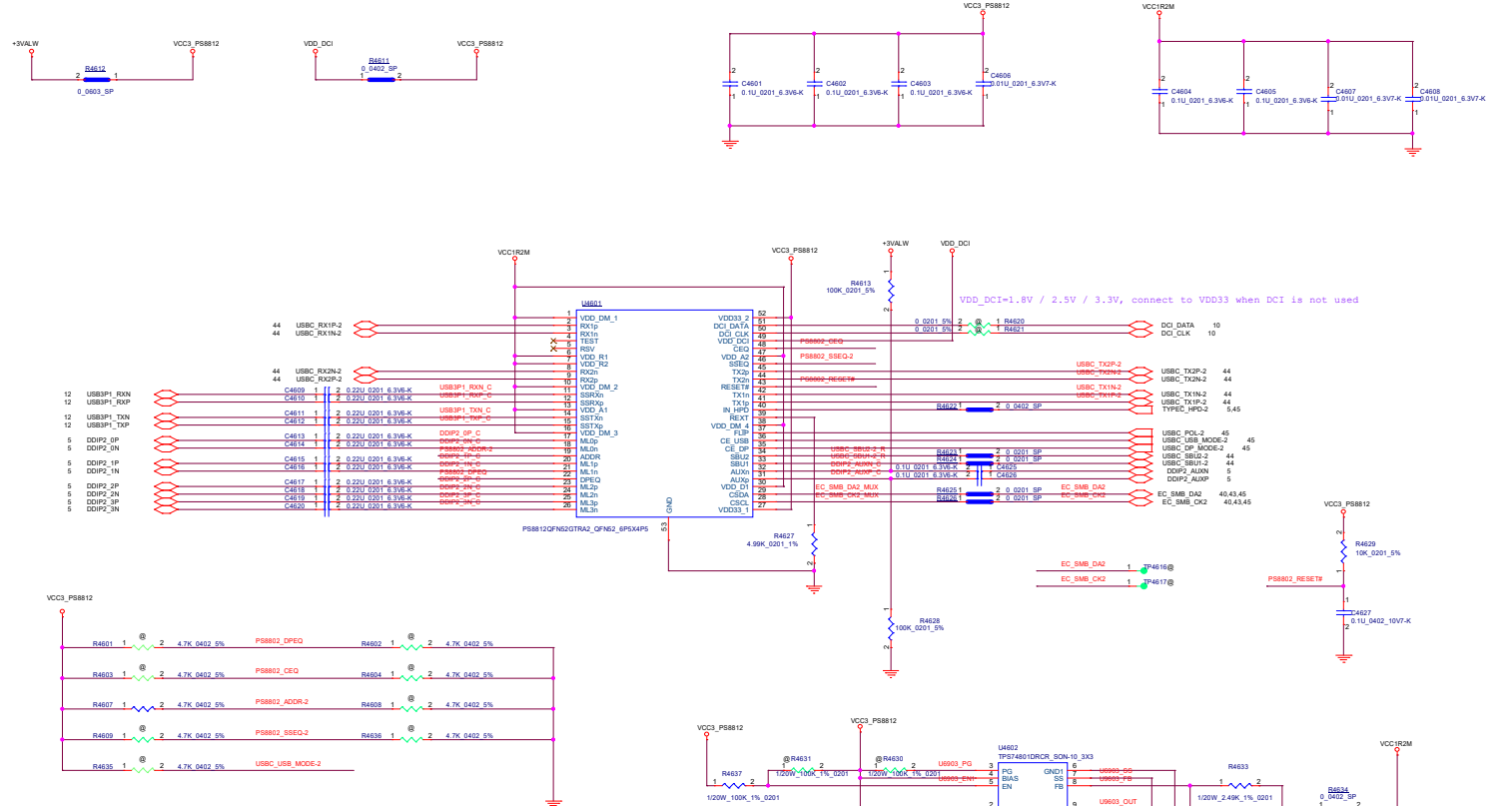
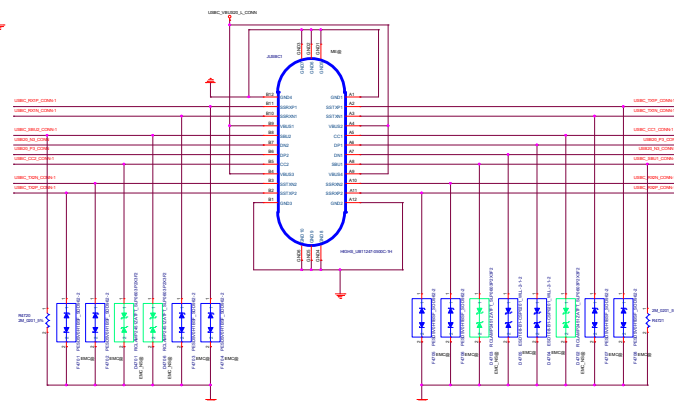
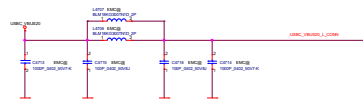
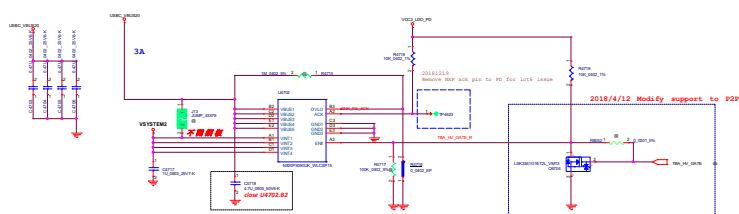


TABLE:

Module Configuration for PS8743 Mode Selection				
State #	CE_DP Pin23 (CTL-1)	CE_USB Pin38 (CTL-0)	FLIP Pin38 (FLIP)	MODE
0	H	H	H	1-port USB on SS2 2-lane DP. DP ML0 is on SSRX1(Flipped)
1	H	H	L	1-port USB on SS1 2-lane DP. DP ML0 is on SSRX2(Un-flipped)
2	H	L	H	4-lane DP. DP ML0 is on SSRX1(Flipped)
3	H	L	L	4-lane DP. DP ML0 is on SSRX2(Un-flipped)
4	L	H	H	1-port USB only on SS2 channels (Flipped)
5	L	H	L	1-port USB only on SS1 channels (Un-flipped)
6	L	L	H	Chip power down
7	L	L	L	Chip power down

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Date	February, March 13, 2015	Drawn	at



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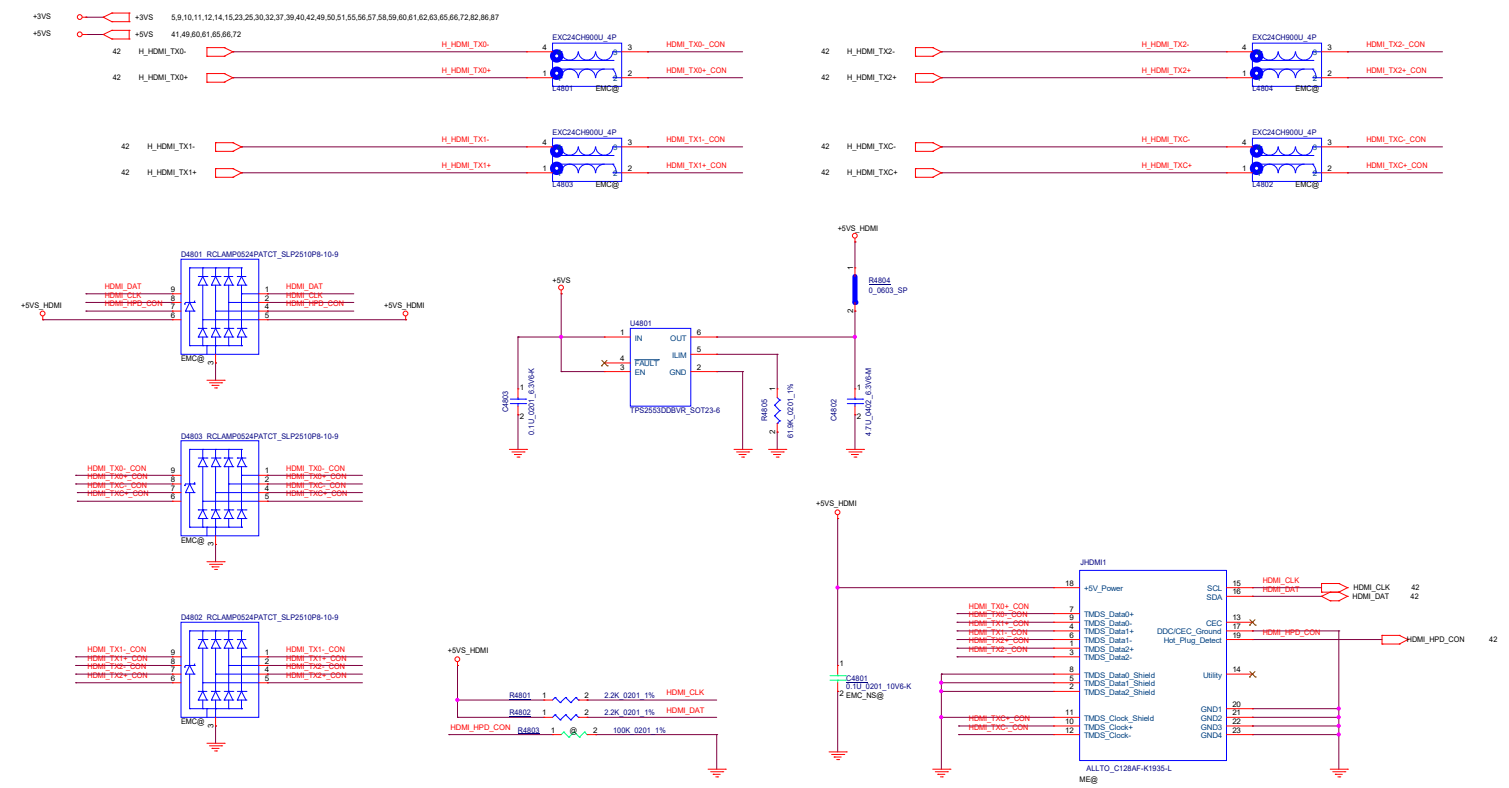
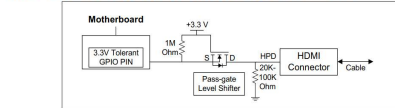


Figure 7-12. HDMI 1.4+ HPD Active Level Shifter Design Recommendation

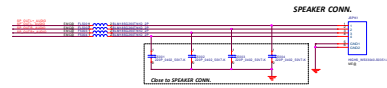
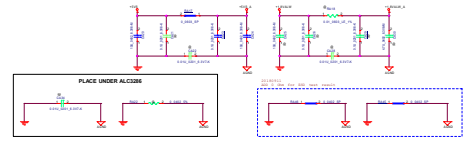
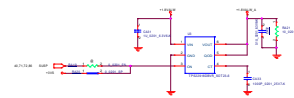
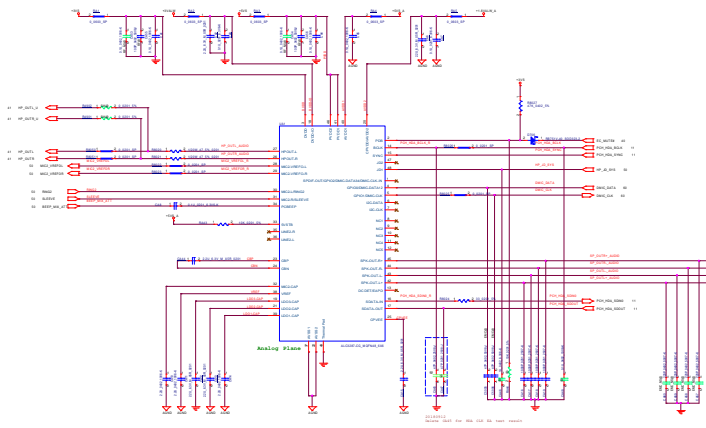
Figure 7-13. HDMI 1.4+ HPD Cost Reduced Level Shifter Design Recommendation



Note: 3.3V transistor gate supply must turn off when CPU power is turned off.

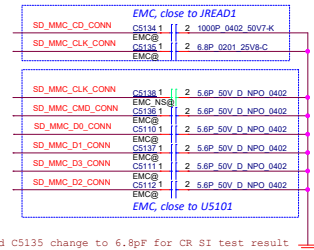
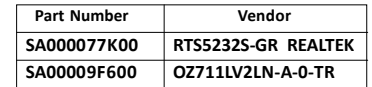
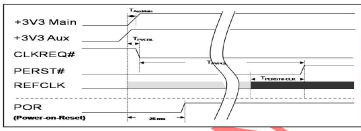
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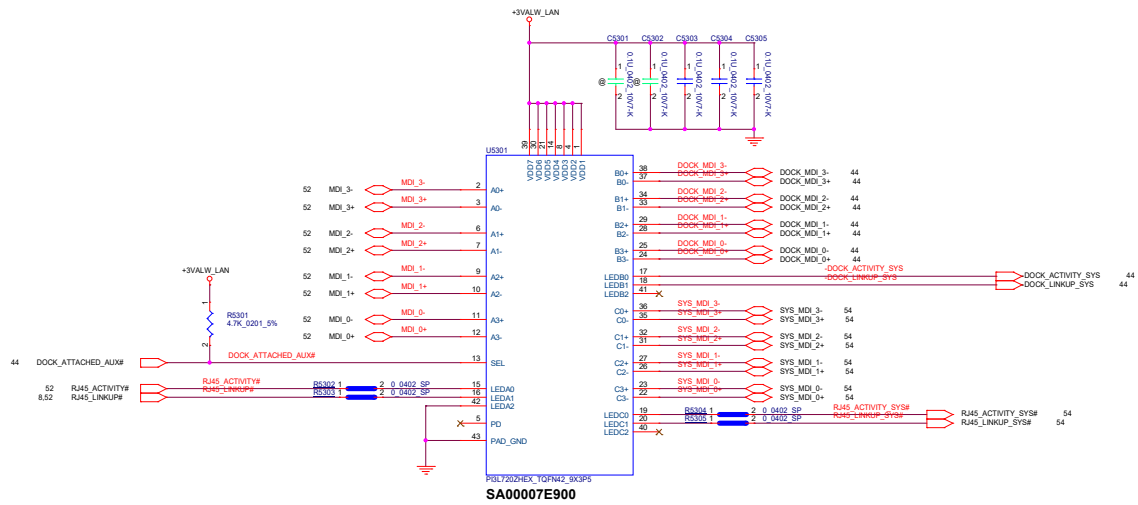
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				Date:	Wednesday, March 13, 2019	ISheet	51 of 99

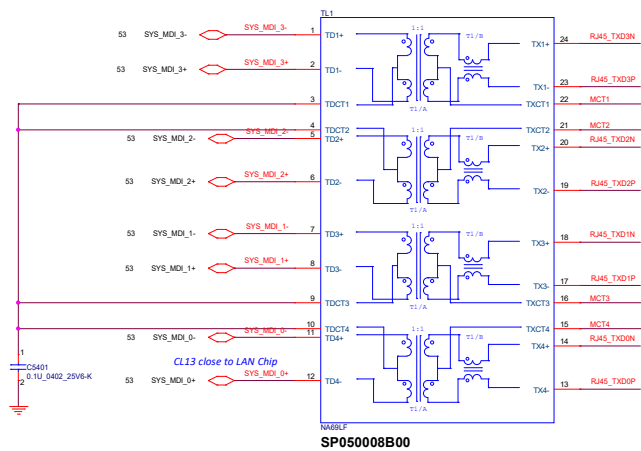




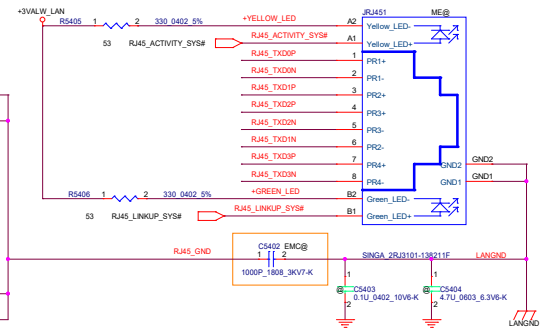
Vendor	P/N	NOTE
Pericom	PI3L7202HE-CX, SA00007E900	Main Source
ONsemi	NCN7201, SA00005TF00	2nd Source (FVT)

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# LAN X' FORM

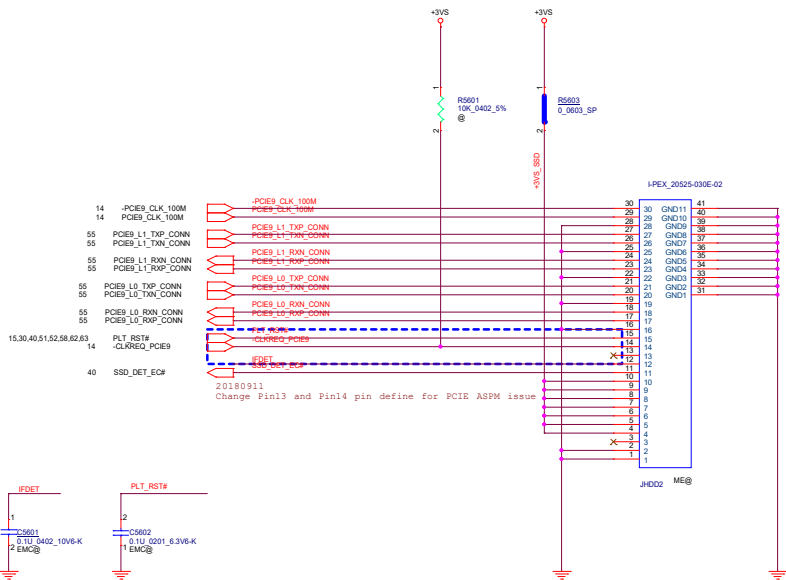


## RJ45 Conn.



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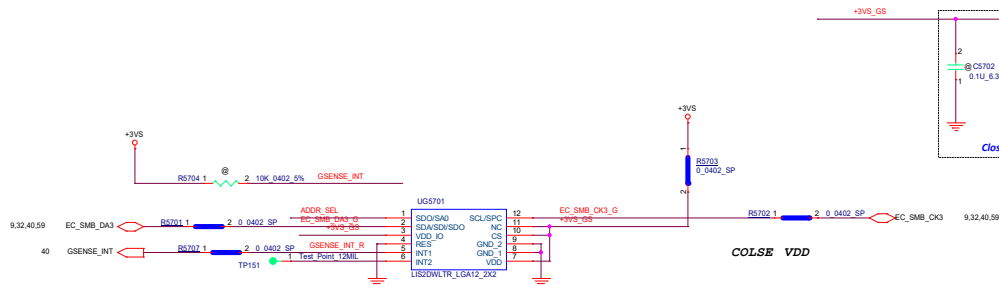




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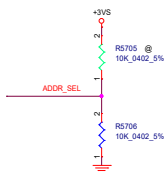
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COLSE VDDIO

COLSE VDD

TABLE of G-Sensor (UG5701)		
Vendor	P/N	LCFC P/N
Kionix	KX022-1020	SA000081E00
ST	LIS2DWLTR	SA00009AQ00



TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

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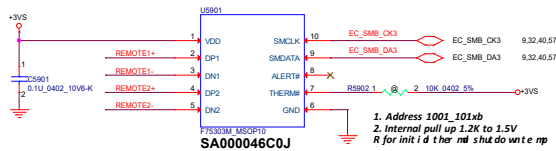
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Size	Document Number	Rev
Custom	<b>FL490/FL590 NM-B931</b>	0.3

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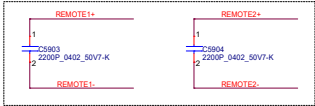


TABLE of Thermal Sensor (U5901)		
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SMC	SA00002921J	S IC EMC1403-2-AIZL-TR MSOP 10P SENSOR

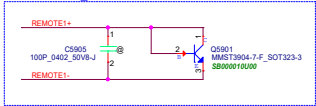
Thermal Sensor



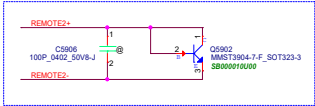
Close to U8




Close to +VCC\_CORE



Close J1DIMM1&J1DIMM2



REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

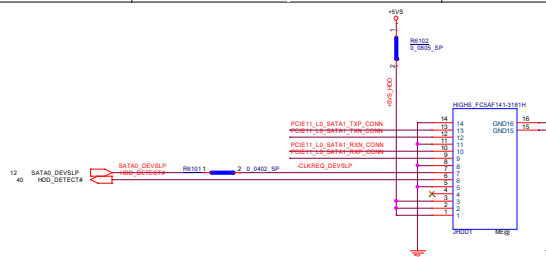
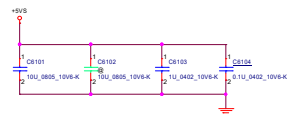
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Issued Date		2015/01/12		Deciphered Date		2016/01/12				
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Size	Document Number	FL490/FL590 NM-B031						Rev	0.3	
Custom	FL490/FL590 NM-B031	Date						Wednesday, March 18, 2015	Sheet	09 of 09



## SATA HDD CONN.

+3V5 41.48,49,50,55,66,72

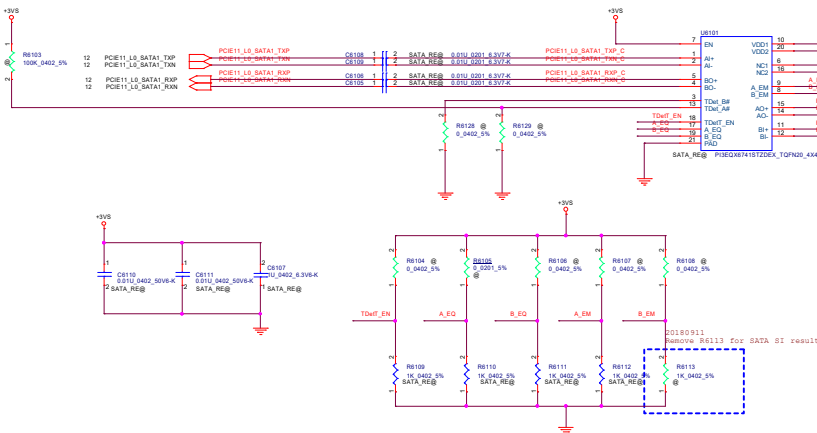
+3V5 5,6,10,11,12,14,15,23,25,30,32,37,39,40,42,49,50,51,55,56,57,58,59,60,62,63,65,66,72,82,86,87



POE11_L0_SATA1_TXP	R8104	2	NSATA_REG @ 0.0201 %	POE11_L0_SATA1_TXP_R	NSATA_REG @ 0.012	1	2	0.01U 0.001 0.3V7-K	POE11_L0_SATA1_TXP_CONN
POE11_L0_SATA1_TXN	R8105	2	NSATA_REG @ 0.0201 %	POE11_L0_SATA1_TXN_R	NSATA_REG @ 0.013	1	2	0.01U 0.001 0.3V7-K	POE11_L0_SATA1_TXN_CONN
POE11_L0_SATA1_RXP	R8106	2	NSATA_REG @ 0.0201 %	POE11_L0_SATA1_RXP_R	NSATA_REG @ 0.014	1	2	0.01U 0.001 0.3V7-K	POE11_L0_SATA1_RXP_CONN
POE11_L0_SATA1_RXN	R8107	2	NSATA_REG @ 0.0201 %	POE11_L0_SATA1_RXN_R	NSATA_REG @ 0.015	1	2	0.01U 0.001 0.3V7-K	POE11_L0_SATA1_RXN_CONN

Pin	Diodes	T1	Comment
3	PIREXQ67A15T	AVCP601	Connect to ground
6	NC	DEW2	Connect to ground and reserve pull-up with 4.7k to 3.3V
13	NC	DEW1	Connect to ground
16	NC	DEW1	Connect to ground and reserve pull-up with 4.7k to 3.3V
18	TDeT_EN	GND	Connect to ground

## SATA REDRIVER



### Configuration Table - Output Pre-emphasis/Swing Setting

A_EM/B_EM	3 Gb/s	6 Gb/s
0	500mV pp	600mV pp
1	500mV pp + 3dB Pre-emphasis	600mV pp + 1.5dB Pre-emphasis

### Configuration Table - Input Equalizer

A_EQ/B_EQ	1.5 Gb/s	3 Gb/s	6Gb/s
0	1 dB	2.5 dB	3 dB
floating	2.5 dB	5 dB	6 dB
1	4 dB	7.5 dB	9 dB

### EL480/580 Setting

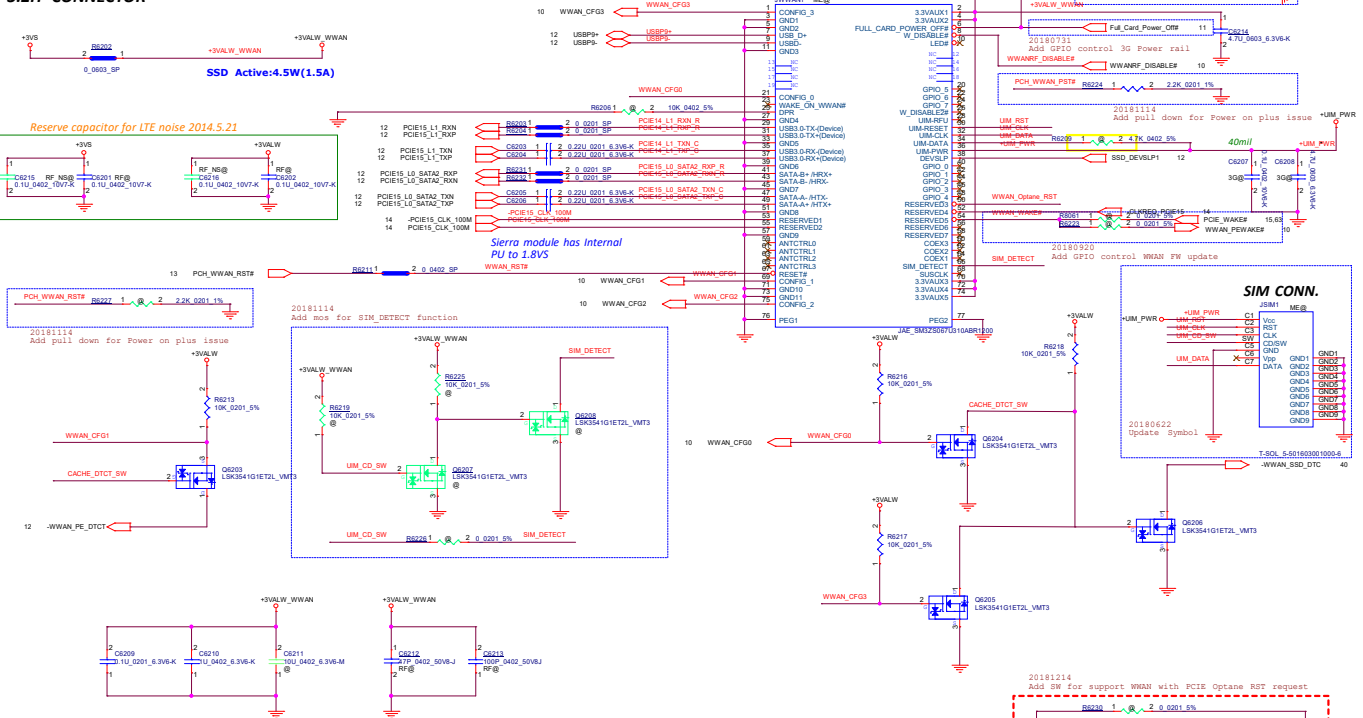
TX EQ	TX EM	RX EQ	RX EM
3dB	0dB	3dB	0dB

KENOBI

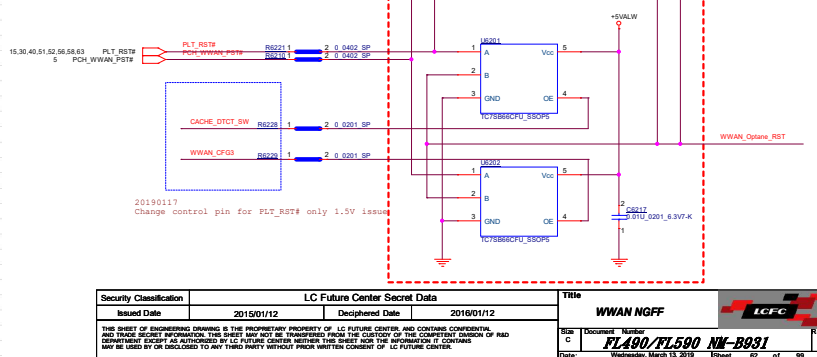
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Doc ID: FL490/FL590 NM-8981			Rev: 1.0

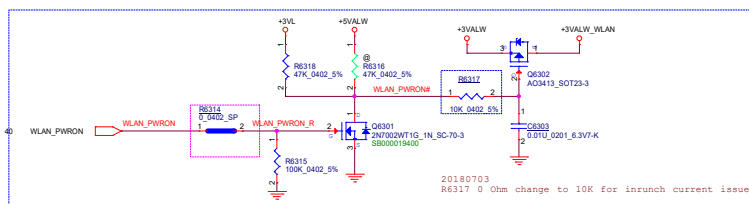
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### TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR



Solo/Lando 2.0 KP list	Part number	GFP_A21 Pin21	GFP_A18 Pin69	GFP_A19 Pin75	GFP_A21 Pin1
		CONFIG 0	CONFIG 1	CONFIG 2	CONFIG 3
Fibocom L850-GL (PCIe or USB2.0 interface)	PK29200T010	GND	GND	GND	NC
Fibocom L830-EB (USB2.0 interface)	PK29200SR20	NC	GND	GND	GND
PCIe 3x2 M.2 2242-83-B-M (PCIe interface)	ED90000F800	GND	NC	GND	GND
SATA MLC M.2 2242-D3		GND	GND	GND	GND
WWAN_CFG3	-WWAN_SSD_DTCT	SSD PCIe WWAN USB2_WWAN			
L	H				
H	H				
L	H				
H	H				
-WWAN_SSD_DTCT					
L(SATA interface)->SATA SSD					
H(PCIe interface)->PCIe SSD (optane Memory					
H(PCIe interface)->USB WWAN /PCIe WWAN					
H(PCIe interface)->沒插任何卡					
-WWAN_FE_DTCT					
L(SATA interface)->SATA SSD					
H(PCIe interface)->PCIe SSD (optane Memory					





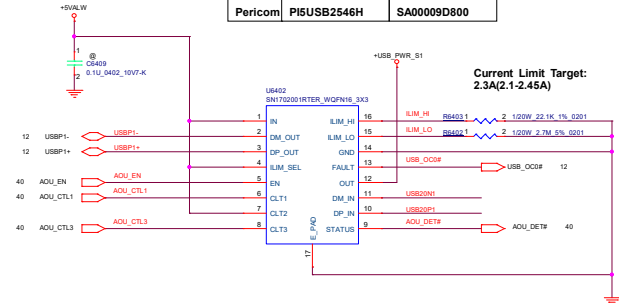
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Issued Date		Deciphered Date		WLAN NGFF CONN.			
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		FL490/FL590 NW-B931		1		01/12/2016	

USB HUB

+5VALW 38.39,40.41,50.52,62.63,66,67,71.72,84,86,87,88,89,90,92,94,95  
+3VS 5,9,10,11,12,14,15,23,25,30,32,37,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,65,66,72,82,86,87

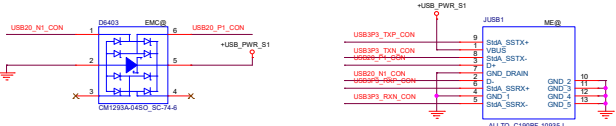
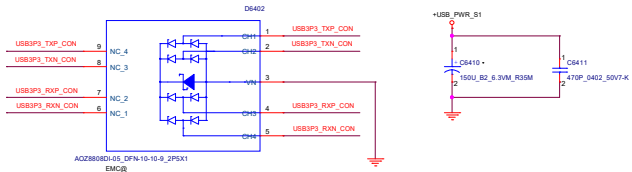
On Board (LEFT-Back)

TABLE of USB Charge		LCFC P/N
TI	SN1702001RTER	SA00008HF00
Pericom	PI5USB2546H	SA00009D800



Current Limit Target:  
2.3A(2.1-2.45A)

CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCR OUT test low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

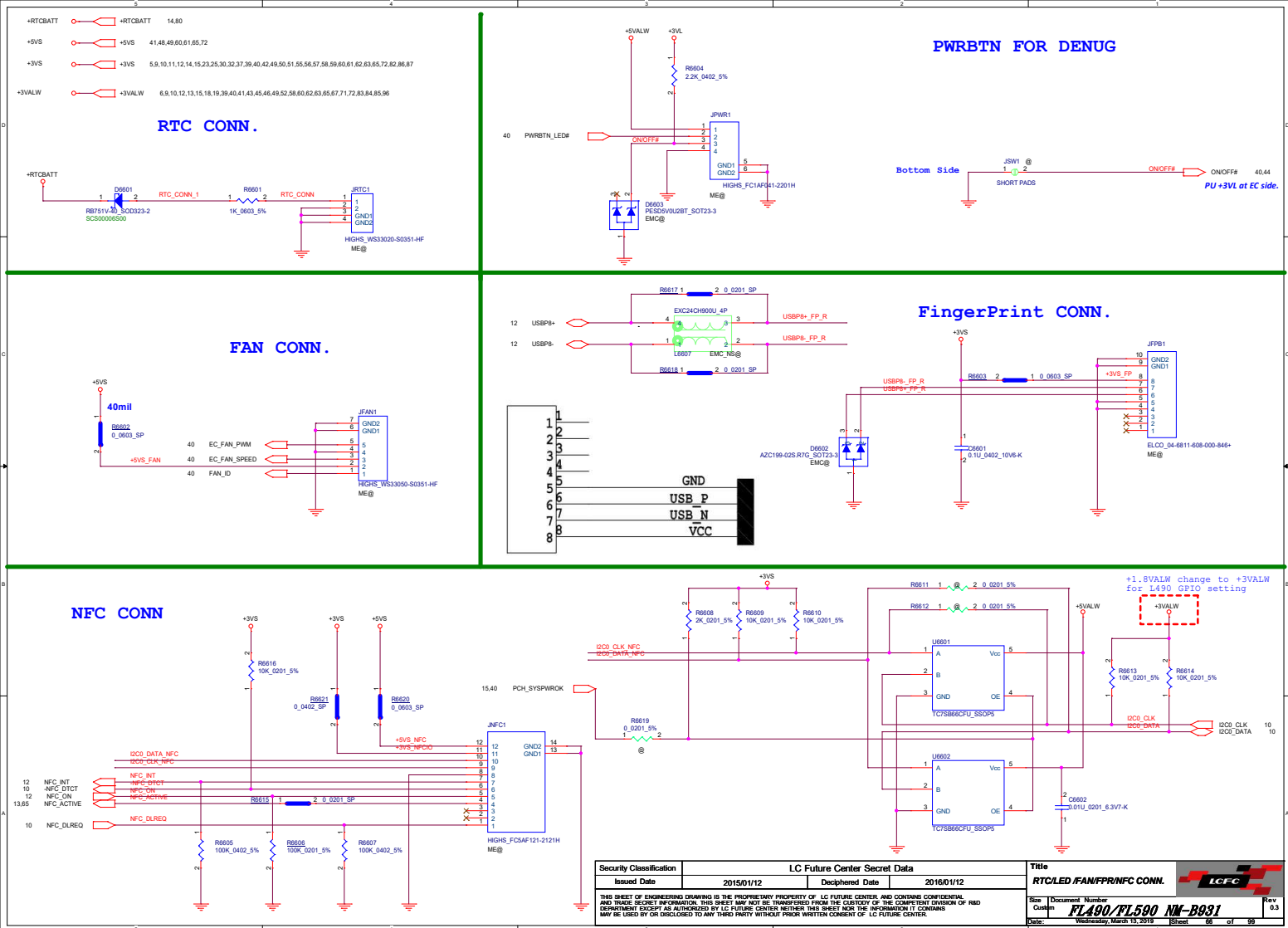


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				FL490/FL590 NM-B931	
				Rev	0.3

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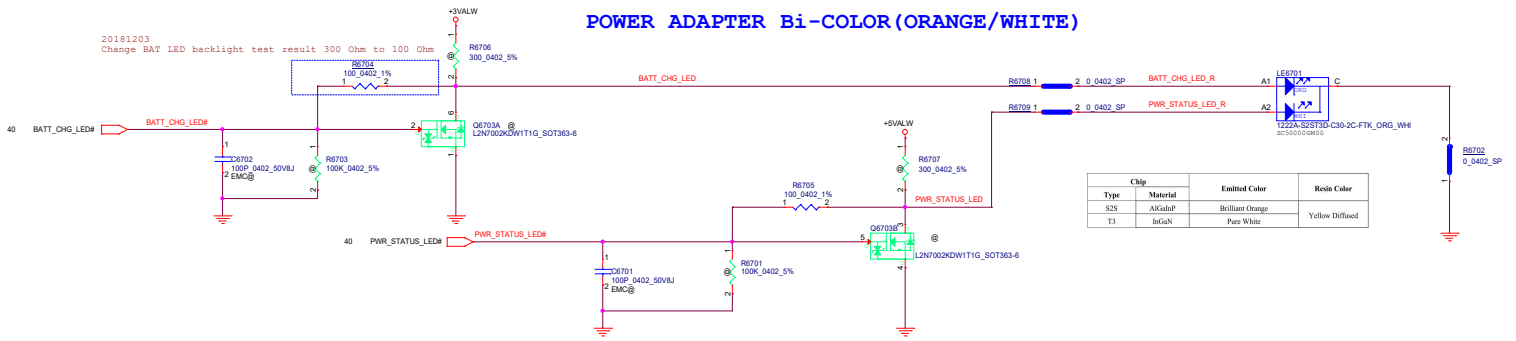






# POWER ADAPTER Bi-COLOR (ORANGE/WHITE)


20181203  
Change BAT LED backlight test result 300 Ohm to 100 Ohm



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				Sheet	87 of 99
				Rev	0.3



THP2

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				Date Wednesday, March 18, 2015
				Sheet 09 of 09
				Rev 0.3





+5VALW		+5VALW	38,39,40,41,50,52,62,63,64,66,67,71,84,86,87,88,89,90,92,94,95
+5VS		+5VS	41,48,49,60,61,65,66
+3VALW		+3VALW	6,8,10,12,13,15,18,19,39,40,41,43,45,46,49,52,58,60,62,63,65,66,67,71,83,84,85,96
+3VS		+3VS	5,9,10,11,12,14,15,23,25,30,32,37,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,65,66,82,86,87
+3VALW_PCH		+3VALW_PCH	5,8,9,10,11,12,13,15,19
+3VL		+3VL	19,40,52,63,65,66,80,82,83,84

## Smart Switch +5VALW To +5VS +3VALW To +3VS

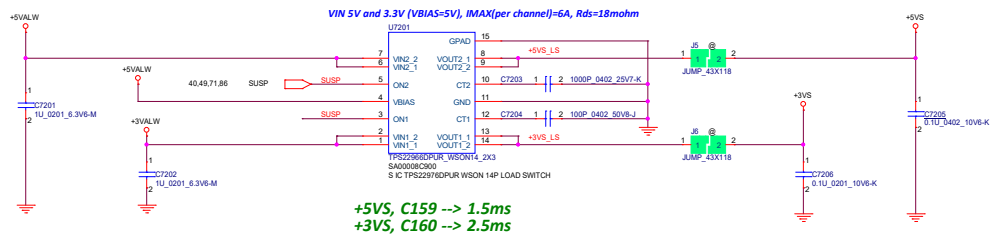
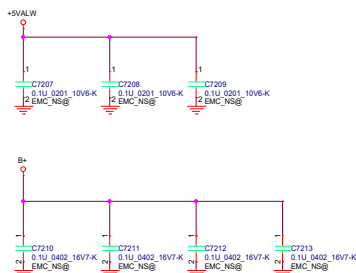


TABLE of POWER SWITCH (U7201)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH



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				Date	Wednesday, March 15, 2015
				Sheet	12 of 99






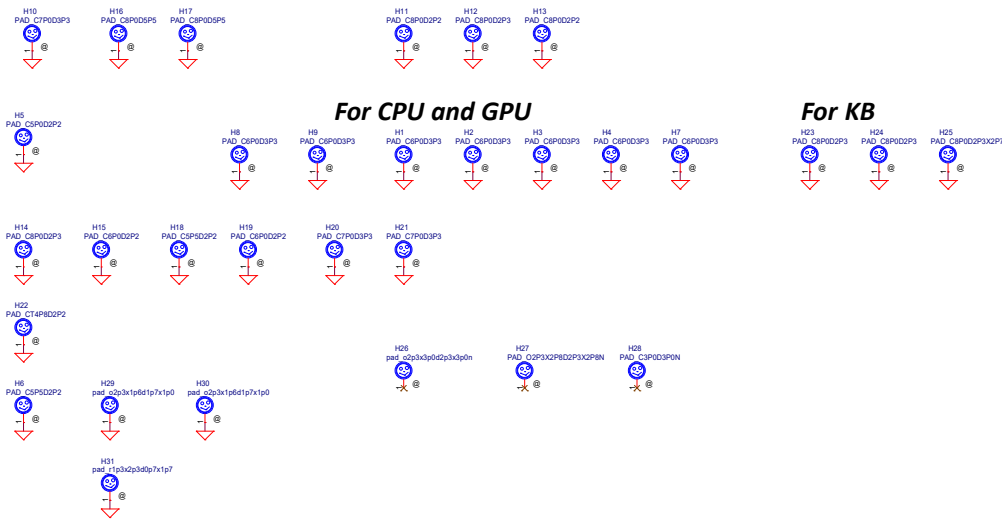
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Date:		Wednesday, March 13, 2019		1 Sheet 76 of 10	

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				Date	Revised, March 13, 2015		Drawn	IT	By	SA

For ME GND hole      Screw Hole




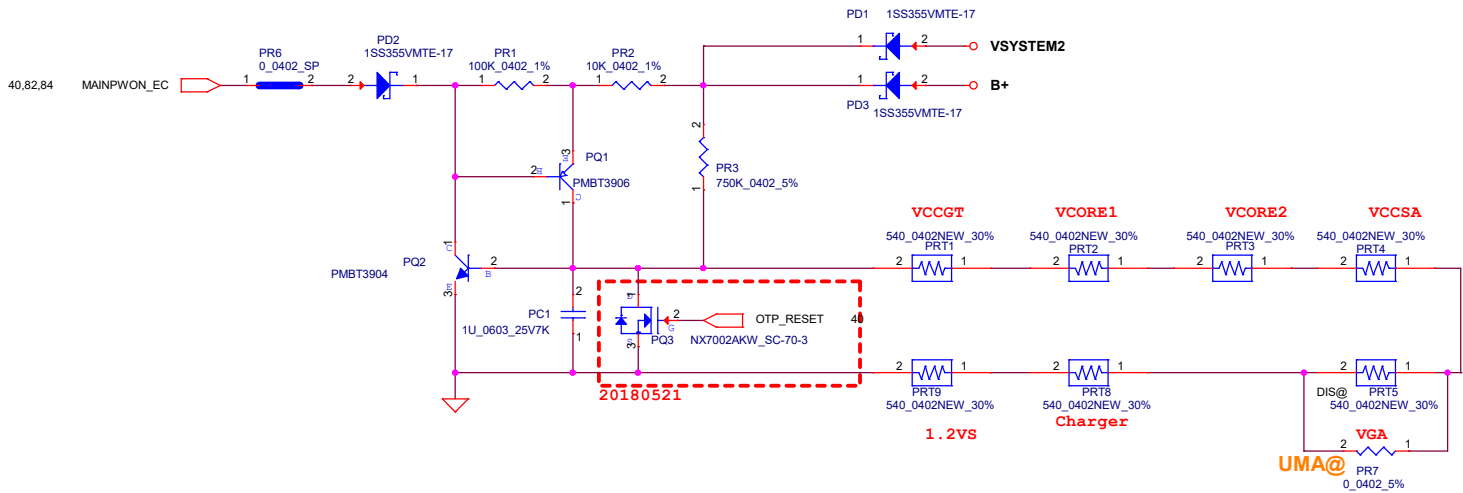
ZZZ1  
NM-B931

PCB Federal Mark PAD

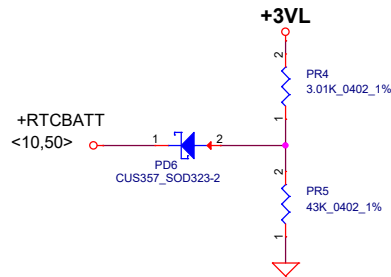


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2015/01/12		2016/01/12		Size	
				Document Number	
				FL490/FL590 NM-B931	
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				Date	
				Wednesday, March 15, 2016	
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				Wednesday, March 15, 2016	Sheet 79 of 99





### RTC Battery

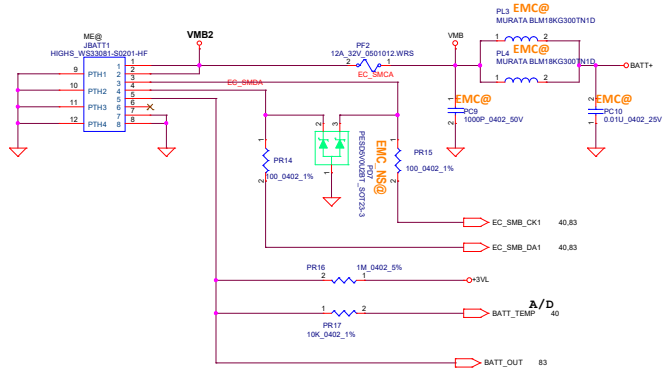


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Date: Wednesday, March 13, 2019				Sheet	80 of 99
				Rev	2.0

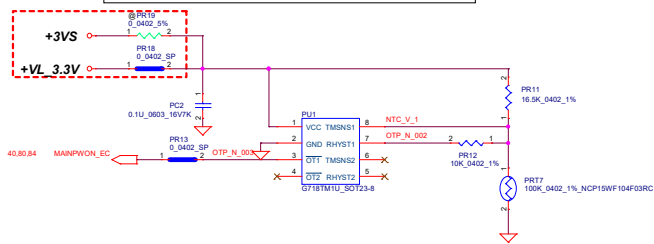


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				3		2.0
				Date:	Wednesday, March 13, 2019	Sheet 81 of 99

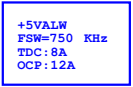
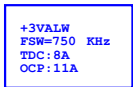


PRT7 under CPU bottom side for CPU thermal protection.  
This is for thermal team request.





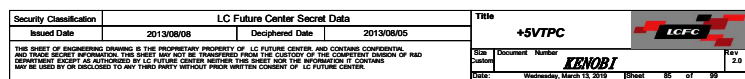
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2013/08/05		2014/12/31		Size	
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		2-00000		2.0	
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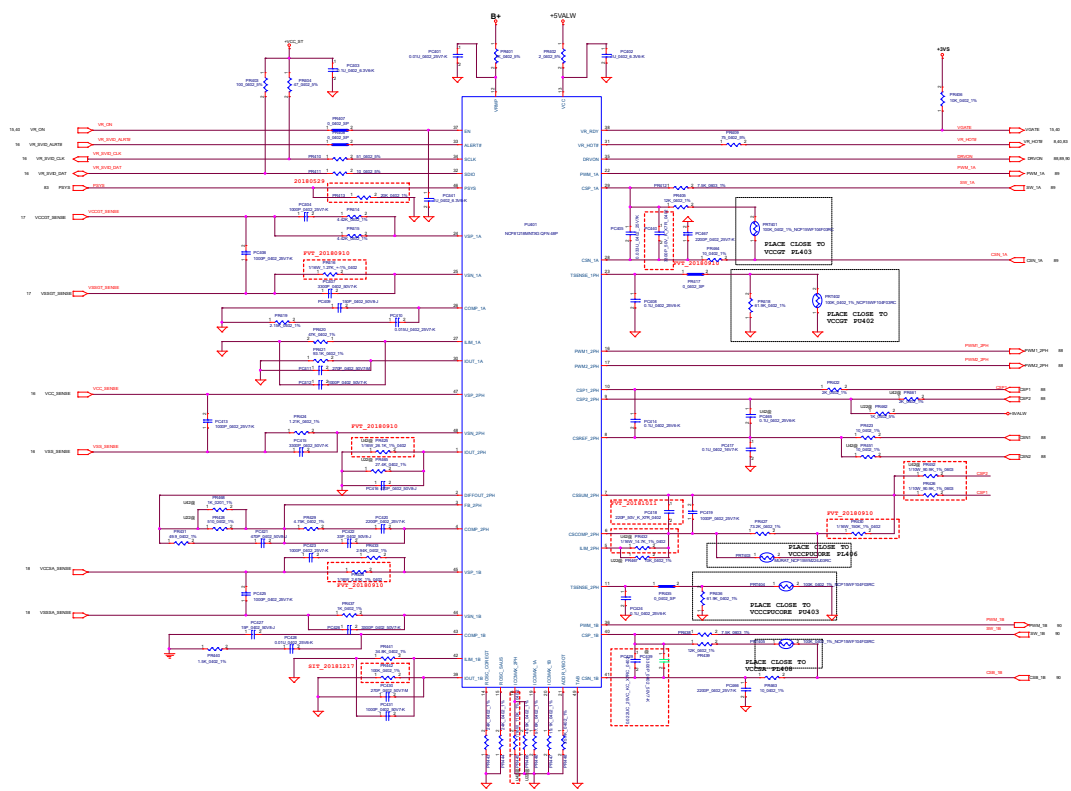


	LV6228C	RT6228A
PR220	NC	0
PR221	0	NC
PC225	4.7U	1U
PR222	0	NC
PR223	NC	0
PR224	0	115K
PR225	NC	15K
PC234	NC	10P
PR226	NC	1K

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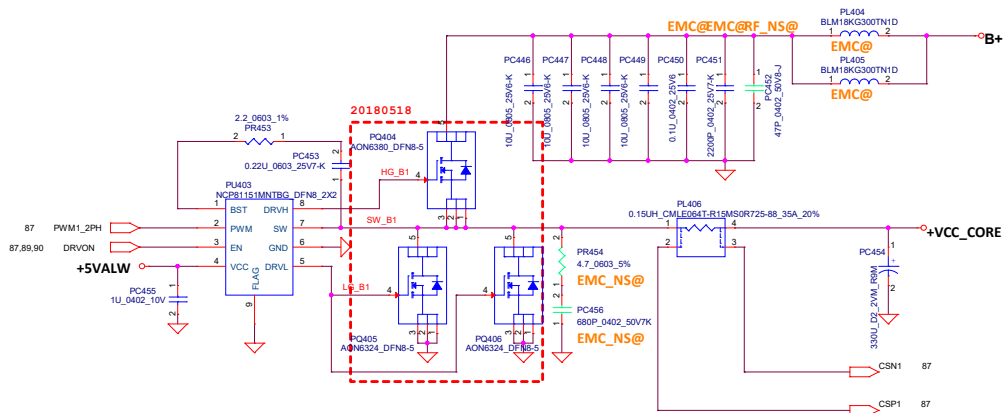






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Project Name	000000	Project Number	000000
Project Manager	000000	Project Engineer	000000
Project Status	000000	Project Date	000000

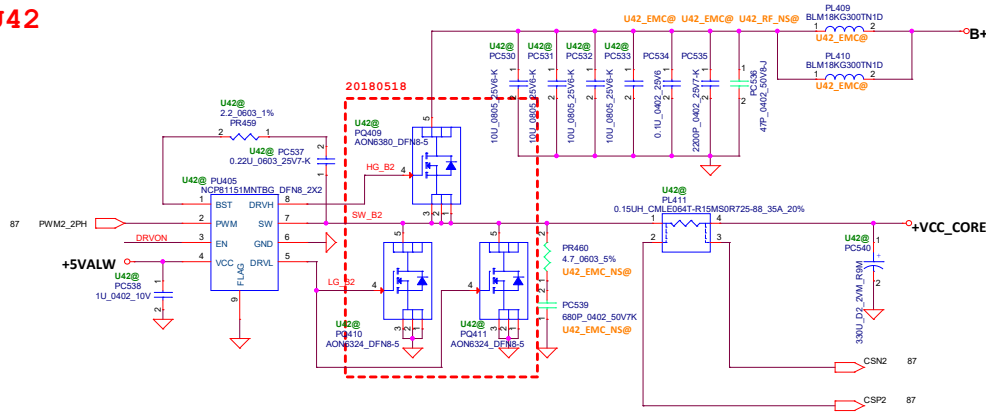
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TDC= 48A  
IccMAX=70A  
OCP=76A

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TDC= 21A  
IccMAX=31A  
OCP= 36A

For U42



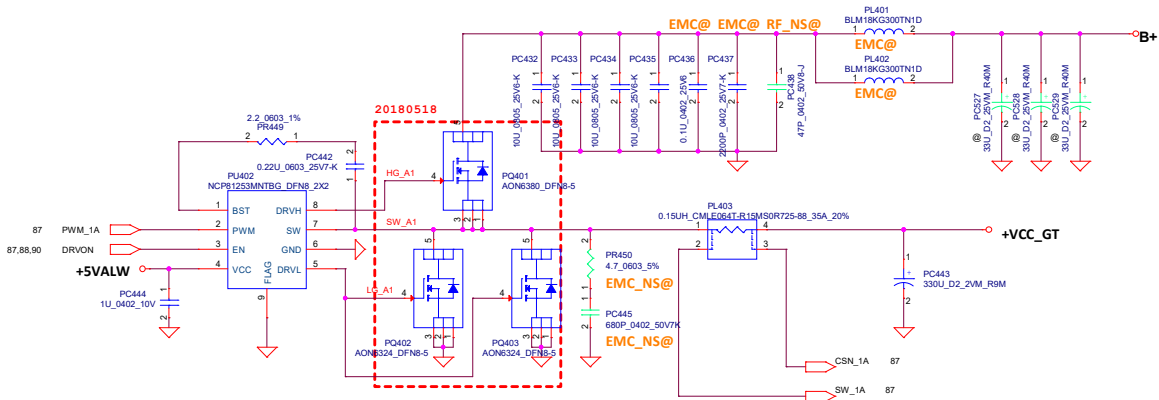
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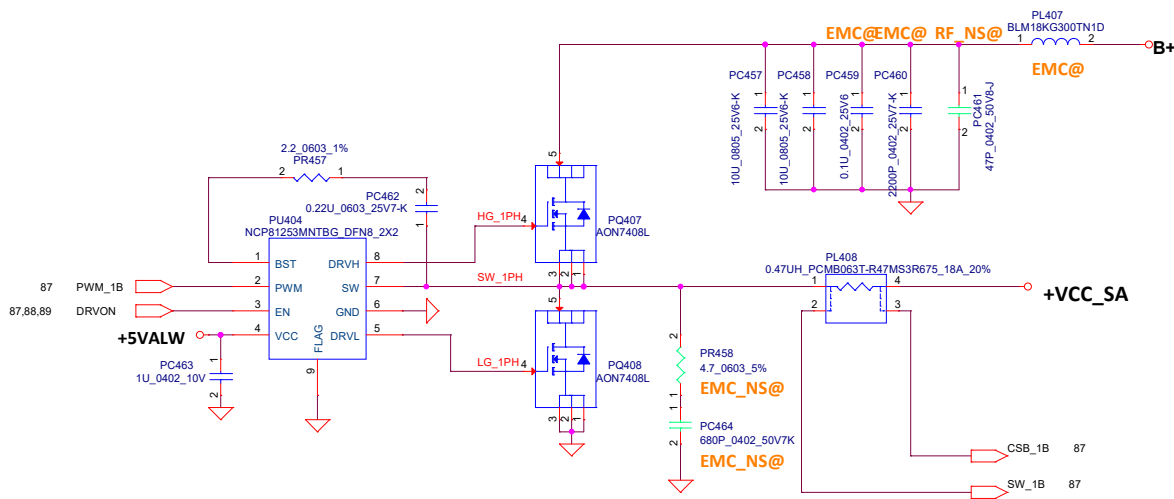


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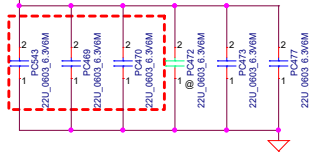
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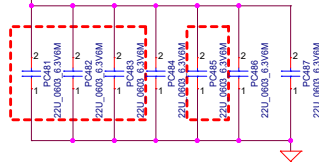
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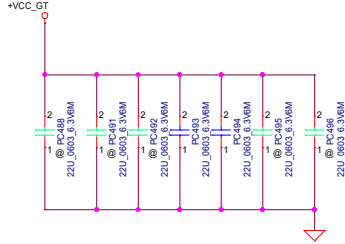
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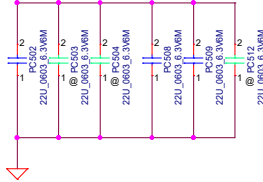
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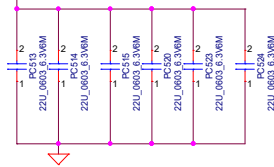
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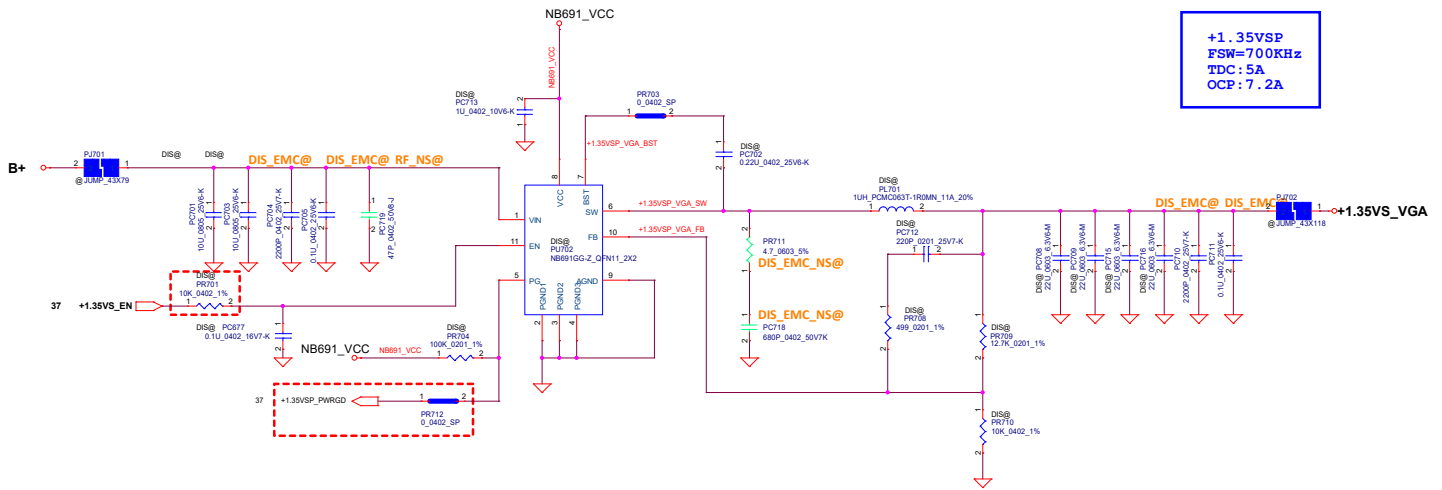
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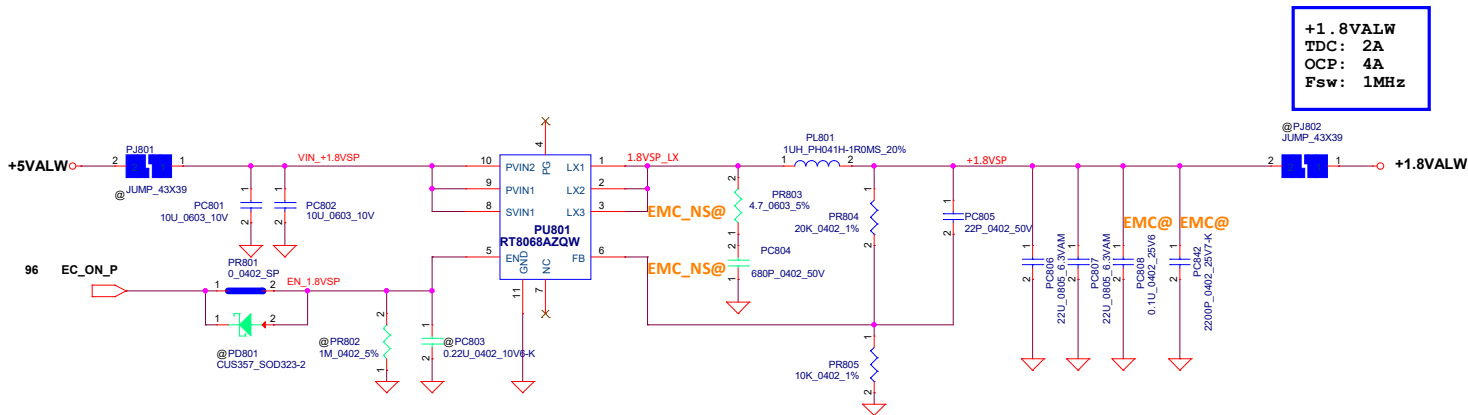
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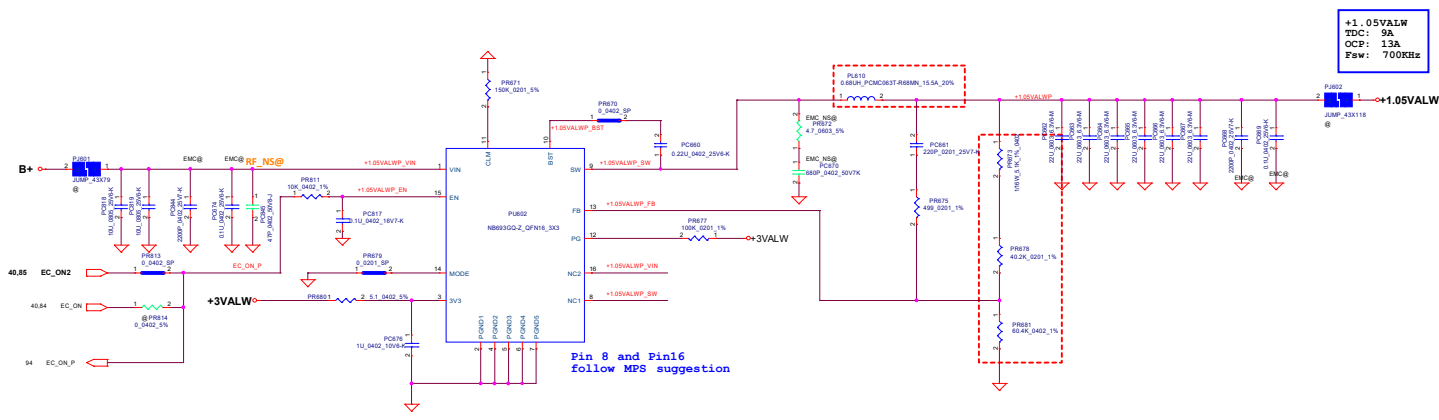


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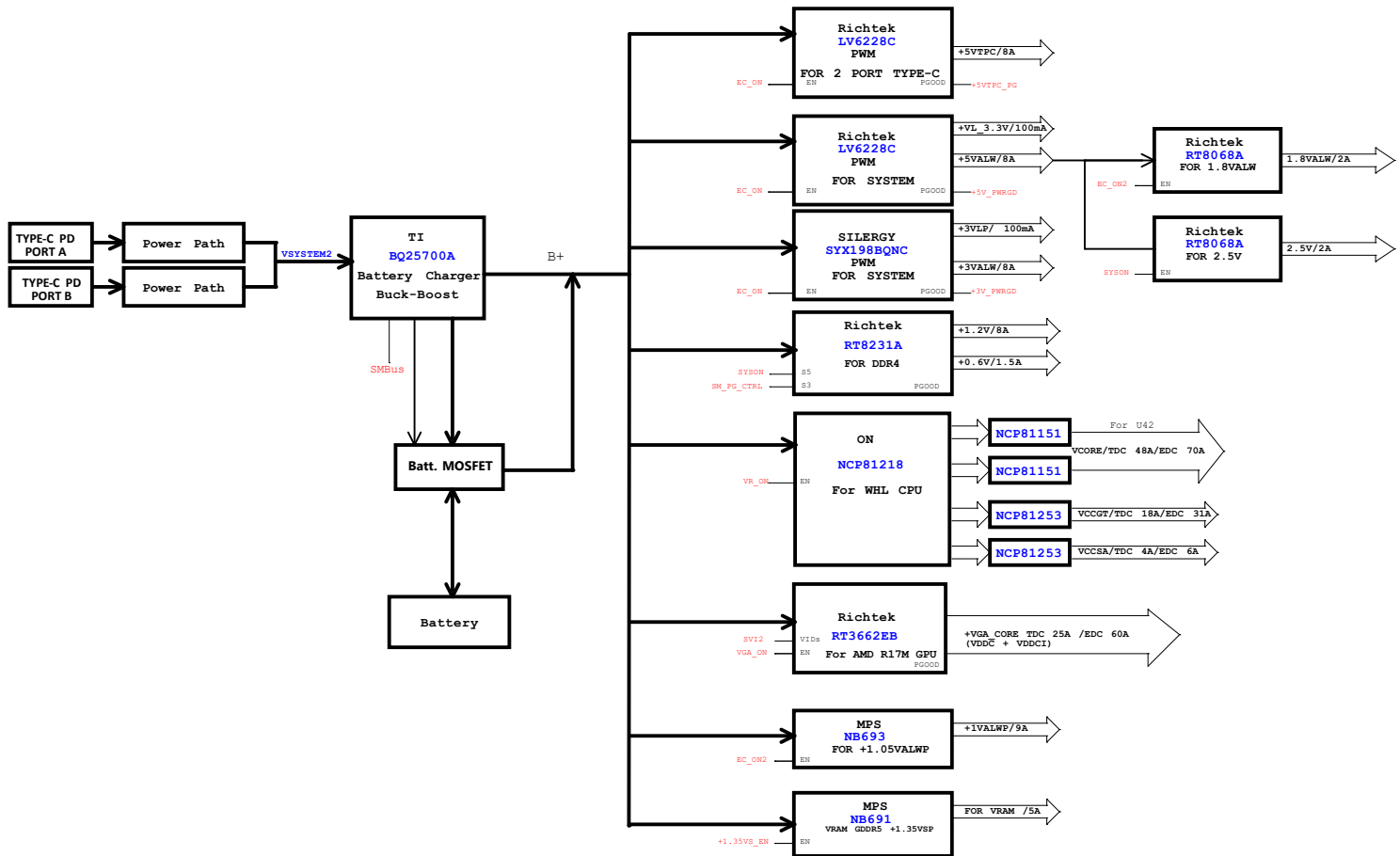
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